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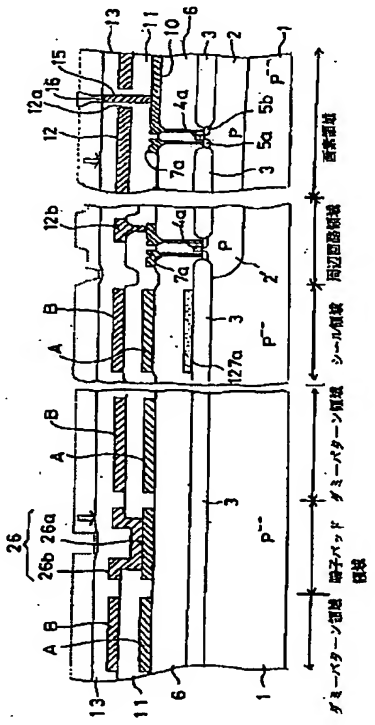
(54)【発明の名称】　電気光学装置用基板、電気光学装置、電子機器及び投写型表示装置

(57)【要約】

【課題】　画素選択用トランジタの素子領域を作り込んだ半導体基板の上に層間絶縁膜とメタル層を交互に繰り返して成膜した積層膜構造を有する液晶パネル用基板において、被研磨膜に係る層間絶縁膜を厚膜化せずに、研磨レートの均一化を達成できる構造を実現する。

【解決手段】　液晶パネル用基板は、画素領域において第２のメタル層からなる遮光膜１２に開けた開口部１２ａを通して遮光膜下の第２の層間絶縁膜１１を挟んで第１のメタル層からなる配線膜１０と遮光膜上の第３の層間絶縁膜１３を挟んで第３のメタル層からなる画素電極とを導電接続する接続プラグ１５を備えている。非画素領域の入力端子パッド２６の周囲に、第１のメタル層からなる下層ダミーパターンＡと第２のメタル層からなる上層ダミーパターンＢが積み重ね形成されている。ダミーパターンＡ，Ｂ上の第３の層間絶縁膜１３の成膜表面レベルが底上げされるため、その部分での過研磨を解消できる。そのため、ＣＭＰ処理において一様の研磨レートが得られる。



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【特許請求の範囲】

【請求項１】　各画素に対応するスイッチング素子が基板上に配置される画素領域において、複数の層間絶縁膜と複数の導電層とが交互に積層された積層膜構造を有しており、該複数の導電層のうちの最上層の導電層より下層の少なくとも一層の前記層間絶縁膜が研磨処理で平坦化されて成る電気光学装置用基板であって、
前記基板上の非画素領域において形成された少なくとも端子パッドの近傍には、前記研磨処理の層間絶縁膜よりも下層の前記導電層からなる単層又は複層のダミーパターンを有して成ることを特徴とする電気光学装置用基板。

【請求項２】　請求項１において、前記端子パッドは基板縁近傍に配置された入力端子パッドであり、前記入力端子パッドの周囲に配置された前記ダミーパターンは平面的に細分化された複数の小分けダミーパターンから成ることを特徴とする電気光学装置用基板。

【請求項３】　請求項２において、相隣り合う前記入力端子パッドの間は非ダミーパターン領域であることを特徴とする電気光学装置用基板。

【請求項４】　請求項３において、前記入力端子パッドとその周囲に配置された前記小分けダミーパターンとの間隔は、配線とその近傍の前記ダミーパターンとの間隔よりも広く設定されて成ることを特徴とする電気光学装置用基板。

【請求項５】　請求項１において、前記端子パッドは基板内方側に配置された中継端子パッドであり、前記中継端子パッドとその周囲に配置された前記ダミーパターンとの間隔は、配線とその近傍の前記ダミーパターンとの間隔よりも広く設定されて成ることを特徴とする電気光学装置用基板。

【請求項６】　各画素に対応するスイッチング素子が基板上に配置される画素領域において、複数の層間絶縁膜と複数の導電層とが交互に積層された積層膜構造を有しており、該複数の導電層のうちの最上層の導電層より下層の少なくとも一層の前記層間絶縁膜が研磨処理で平坦化されて成る電気光学装置用基板であって、
前記画素領域の周囲に形成されるシール領域には、前記研磨処理の層間絶縁膜よりも下層の前記導電層からなる単層又は複層のダミーパターンを有して成ることを特徴とする電気光学装置用基板。

【請求項７】　各画素に対応するスイッチング素子が基板上に配置される画素領域において、複数の層間絶縁膜と複数の導電層とが交互に積層された積層膜構造を有しており、該複数の導電層のうちの最上層の導電層より下層の少なくとも一層の前記層間絶縁膜が研磨処理で平坦化されて成る電気光学装置用基板であって、
前記画素領域の周囲に形成されるシール領域の外側の外周領域には、前記研磨処理の層間絶縁膜よりも下層の前記導電層からなる単層又は複層のダミーパターンを有して成ることを特徴とする電気光学装置用基板。

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【請求項８】　請求項６又は請求項７において、前記ダミーパターンは、前記スイッチング素子の制御配線層と同層で形成された孤立パターンの上に積み足されて成ることを特徴とする電気光学装置用基板。

【請求項９】　各画素に対応するスイッチング素子が基板上に配置される画素領域において、複数の層間絶縁膜と複数の導電層とが交互に積層された積層膜構造を有しており、該複数の導電層のうちの最上層の導電層より下層の少なくとも一層の前記層間絶縁膜が研磨処理で平坦化されて成る電気光学装置用基板であって、
前記画素領域の周辺に配置され前記スイッチング素子に信号を供給する駆動回路の近傍領域には、前記研磨処理の層間絶縁膜よりも下層の前記導電層からなる単層又は複層のダミーパターンを有して成ることを特徴とする電気光学装置用基板。

【請求項１０】　各画素に対応するスイッチング素子が基板上に配置される画素領域において、複数の層間絶縁膜と複数の導電層とが交互に積層された積層膜構造を有しており、該複数の導電層のうちの最上層の導電層より下層の少なくとも一層の前記層間絶縁膜が研磨処理で平坦化されて成る電気光学装置用基板であって、
前記画素領域の周囲に形成されるシール領域の隅部領域には、該シール領域の辺領域又は当該隅部の周辺領域よりも密度の低い分布であり、前記研磨処理の層間絶縁膜よりも下層の前記導電層からなる単層又は複層のダミーパターンを有して成ることを特徴とする電気光学装置用基板。

【請求項１１】　各画素に対応するスイッチング素子が基板上に配置される画素領域において、複数の層間絶縁膜と複数の導電層とが交互に積層された積層膜構造を有しており、該複数の導電層のうちの最上層の導電層より下層の少なくとも一層の前記層間絶縁膜が研磨処理で平坦化されて成る電気光学装置用基板であって、
前記画素領域の周囲に形成されるシール領域には、その隅部領域を除き、前記研磨処理の層間絶縁膜よりも下層の前記導電層からなる単層又は複層のダミーパターンを有して成ることを特徴とする電気光学装置用基板。

【請求項１２】　各画素に対応するスイッチング素子が基板上に配置される画素領域において、複数の層間絶縁膜と複数の導電層とが交互に積層された積層膜構造を有しており、該複数の導電層のうちの最上層の導電層より下層の少なくとも一層の前記層間絶縁膜が研磨処理で平坦化されて成る電気光学装置用基板であって、
前記基板上の非画素領域において前記研磨処理の層間絶縁膜よりも下層の前記導電層を含む複数の擬似画素凹凸パターンを有して成ることを特徴とする電気光学装置用基板。

【請求項１３】　請求項１５において、前記擬似画素凹凸パターンは前記基板上の２次元方向に繰り返し展開形

成されて成ることを特徴とする電気光学装置用基板。

【請求項１４】　請求項１２又は請求項１３において、前記スイッチング素子に電気的に接続する第１の前記導電層と前記研磨処理の層間絶縁膜の上に成膜された上層の前記導電層とが電気的に接続されており、前記第１の導電層と前記上層の前記導電層との中間に第２の前記導電層を含み、

前記擬似画素凹凸パターンは、前記第１の導電層からなる第１のダミーパターン及び前記第２の導電層からなる第２のダミーパターンのいずれか又は両者の積み重ねであることを特徴とする電気光学装置用基板。

【請求項１５】　請求項１７において、前記擬似画素凹凸パターンは少なくとも擬似ゲート線及び擬似データ線で構成されて成ることを特徴とする電気光学装置用基板。

【請求項１６】　請求項１乃至請求項１５のいずれか一項に規定する電気光学装置用基板とこれに対向する透明基板との間隔に電気光学材料を挟持して成ることを特徴とする電気光学装置。

【請求項１７】　請求項１６に規定する電気光学装置を表示部に用いて成ることを特徴とする電子機器。

【請求項１８】　請求項１６に規定する電気光学装置をライトバルブに用いて成ることを特徴とする投写型表示装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、反射型液晶パネル用基板等の電気光学装置用基板に関し、特に、画素選択用素子領域の上に画素領域を積層した電気光学装置用基板に関する。

【０００２】

【関連の技術】本出願人は、１９９６年１０月２２日付出願に係る特願平８－２７９３８８号を以て、以下に述べる液晶パネル用基板，液晶パネル及び投写型表示装置の構成を開示した。反射型液晶パネルをライトバルブとして用いた投写型表示装置（液晶プロジェクタ）は、図１７に示すように、システム光軸L_0に沿って配置した光源部１１０、インテグレータレンズ１２０、及び偏光変換素子１３０から概略構成される偏光照明装置１００と、偏光照明装置１００から射出されたＳ偏光束をＳ偏光束反射面２０１により反射させる偏光ビームスプリッタ２００と、偏光ビームスプリッタ２００のＳ偏光束反射面２０１から反射された光のうち青色光（Ｂ）の成分を分離するダイクロイックミラー４１２と、分離された青色光（Ｂ）を変調する反射型液晶ライトバルブ３００Ｂと、ダイクロイックミラー４１２によって青色光が分離された後の光束のうち赤色光（Ｒ）の成分を反射させて分離するダイクロイックミラー４１３と、分離された赤色光（Ｒ）を変調する反射型液晶ライトバルブ３００Ｒと、ダイクロイックミラー４１３を透過する残りの緑色光（Ｇ）を変調する反射型液晶ライトバルブ３００Ｇと、３つの反射型液晶ライトバルブ３００Ｒ，３００Ｇ，３００Ｂにて変調された光を光路逆進させてダイクロイックミラー４１３，４１２，偏光ビームスプリッタ２００にて合成し、この合成光をスクリーン６００へ投写する投写レンズからなる投写光学系５００とから構成されている。各反射型液晶ライトバルブ３００Ｒ，３００Ｇ，３００Ｂには、それぞれ図１８の断面図に示すような反射型液晶パネル３０が用いられている。

【０００３】この反射型液晶パネル３０は、ガラス又はセラミック等からなる支持基板３２上に接着剤で固着された反射型液晶パネル用基板３１と、この反射型液晶パネル用基板３１上をシール材３６で枠形状に囲み、間隔をおいて対向配置した透明導電膜（ＩＴＯ）からなる対向電極（共通電極）３３を持つ光入射側のガラス基板３５と、反射型液晶パネル用基板３１とガラス基板３５との間のシール材３６で封止された隙間内において充填された周知のＴＮ（Twisted Nematic ）型液晶又は電圧無印加状態で液晶分子が略垂直配向するＳＨ（Super Homeotropic ）型液晶３７とを有している。

【０００４】この反射型液晶パネル３０に用いられる反射型液晶パネル用基板３１の拡大した平面レイアウトを図１９に示す。反射型液晶パネル用基板３１は、図１８に示す多数の画素電極１４がマトリクス状に配置された矩形の画素領域（表示領域）２０と、画素領域２０の左右辺の外側に位置し、ゲート線（走査電極，行電極）を走査するゲート線駆動回路（Ｙドライバ）２２Ｒ，２２Ｌと、画素電極１４の上辺の外側に位置し、データ線（信号電極，列電極）についてのプリチャージ及びテスト回路２３と、画素電極１４の下辺の外側に位置し、データ線に画像データに応じた画像信号を供給する画像信号サンプリング回路２４と、ゲート線駆動回路２２Ｒ，２２Ｌ，プリチャージ及びテスト回路２３，及び画像信号サンプリング回路２４の外側には前述したシール材３７が位置決めされる枠形状のシール領域２７と、下側端に沿って配列されており、異方性導電膜（ＡＣＦ）３８を介してフレキシブルテープ配線３９に固着接続される複数の端子パッド２６と、この端子パッド２６の列とシール領域２７との間に位置し、データ線に対し画像データに応じた画像信号を供給するデータ線駆動回路（Ｘドライバ）２１と、そのデータ線駆動回路２１の両脇に位置し、ガラス基板３５の対向電極３３に給電するための中継端子パッド（いわゆる銀点）２９Ｒ，２９Ｌとから構成されている。

【０００５】なお、シール領域２７の内側に位置する周辺回路（ゲート線駆動回路２２Ｒ，２２Ｌ，プリチャージ及びテスト回路２３，及び画像信号サンプリング回路２４）にも、光が入射するのを防止するため、最上層の画素電極１４と同層の遮光膜２５（図１８参照）が設けられている。

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【０００６】図２０は反射型液晶パネル用基板３１の画素領域２０の一部を拡大して示す平面図で、図２１は図２０中のＡ－Ａ′に沿って切断した状態を示す切断図である。図２０において、１は単結晶シリコンのＰ⁻⁻型半導体基板（Ｎ⁻⁻型半導体基板でも良い）で、２０㎜角の大形サイズである。２はこの半導体基板１のうち素子（ＭＯＳＦＥＴなど）形成領域の表面（主面）側に形成されたＰ型ウェル領域、３は半導体基板１の素子非形成領域における素子分離用に形成されたフィールド酸化膜（いわゆるＬＯＣＯＳ）である。図２１に示すＰ型ウェル領域２は、例えば画素数７６８×１０２４というような画素がマトリクス状に配置された画素領域２０の共通ウェル領域として形成されており、周辺回路（ゲート線駆動回路２２Ｒ，２２Ｌ，プリチャージ及びテスト回路２３，画像信号サンプリング回路２４，及びデータ駆動回路２１）を構成する素子を作り込む部分のＰ型ウェル領域２′（図２２参照）とは分離されている。

【０００７】フィールド酸化膜３には１画素毎の区画領域に２つの開口部が形成されている。一方の開口部の内側中央にゲート絶縁膜４ｂを介して形成されたポリシリコン又はメタルシリサイド等からなるゲート電極４ａと、このゲート電極４ａの両側のＰ型ウェル領域２の表面に形成されたＮ⁺型ソース領域５ａ，Ｎ⁺型ドレイン領域５ｂとは画素選択用のＮチャネル型ＭＯＳＦＥＴ（絶縁ゲート型電界効果トランジスタ）を構成している。行方向に隣接する複数の画素の各ゲート電極４ａは走査線方向（画素行方向）に延在してゲート線４を構成している。

【０００８】また、他方の開口部の内側のＰ型ウェル領域２の表面に形成された行方向共通のＰ型容量電極領域８と、このＰ型容量電極領域８の上に絶縁膜（誘電膜）９ｂを介して形成されたポリシリコン又はメタルシリサイド等からなる容量電極９ａとは画素選択用ＭＯＳＦＥＴで選択された信号を保持するための保持容量Ｃを構成している。

【０００９】ゲート電極４ａ及び容量電極９ａの上には第１の層間絶縁膜６が形成され、この絶縁膜６上にはアルミニウムを主体とする第１のメタル層が形成されている。

【００１０】第１のメタル層には、列方向に延在するデータ線７（図２０参照），データ線７から櫛歯状に突出してコンタクトホール６ａを介してソース領域４ｂに導電接触するソース電極配線７ａ，コンタクトホール６ｂを介してドレイン領域５ｂに導電接触すると共にコンタクトホール６ｃを介して容量電極９ａに導電接触する中継配線１０とが含まれる。

【００１１】データ線７，ソース電極配線７ａ及び中継配線１０を構成する第１のメタル層の上には第２の層間絶縁膜１１が形成され、この第２の層間絶縁膜１１上にはアルミニウムを主体とする第２のメタル層が形成されている。この第２のメタル層は画素領域２０の一面を覆う遮光膜１２が含まれる。なお、この遮光膜１２を構成する第２のメタル層は、画素領域２０の周囲に形成される周辺回路（ゲート線駆動回路２２Ｒ，２２Ｌ，プリチャージ及びテスト回路２３，画像信号サンプリング回路２４，及びデータ駆動回路２１）において素子間の接続用配線１２ｂ（図２２参照）を構成する。

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【００１２】遮光膜１２の中継配線１０に対応する位置にはプラグ貫通用開口部１２ａが開けられている。遮光膜１２の上には第３の層間絶縁膜１３が形成され、この第３の層間絶縁膜１３の上に略１画素分に対応した矩形状の反射電極としての画素電極１４が形成されている。遮光膜１２の開口部１２ａに対応してその内側に位置するように、第３，第２の層間絶縁膜１３，１１を貫通するコンタクトホール１６が設けられている。このコンタクトホール１６内にはタングステン等の高融点金属をＣＶＤ法により埋め込んだ後、第３の層間絶縁膜１３の上に堆積した高融点金属層と第３の層間絶縁膜１３の表面側をＣＭＰ（化学的機械研磨）法で削り込んで鏡面様に平坦化する。次いで、例えば低温スパッタ法によりアルミニウム層を成膜し、パターニングにより一辺が１５～２０μｍ程度の矩形状の画素電極１４を形成する。中継配線１０と画素電極１４とは柱状の接続プラグ（層間導電部）１５で電気的に接続されている。そして、画素電極１４の上にはパッシベーション膜１７が全面的に形成されている。

【００１３】なお、接続プラグ１５の形成方法としては、ＣＭＰ法で第３の層間絶縁膜１３を平坦化した後、コンタクトホールを開口し、その中にタングステン等の高融点金属を埋め込む方法もある。

【００１４】このような第３の層間絶縁膜１３に対するＣＭＰ法による平坦化処理は、その上に成膜される反射電極としての表面鏡面様の画素電極１４を画素毎に成膜するための必須プロセスである。また、画素電極１４の上に保護膜を介して誘電体ミラー膜を形成する場合でも必要となる。このＣＭＰ法は、スクライブ前のウエハを化学的なエッチングと機械的な研磨とを併せて進行せしめる成分からなるスラリー（砥液）を用いて研磨する手法である。

【００１５】ところが、画素領域２０では、画素選択用ＭＯＳＦＥＴや保持容量Ｃの電極配線７ａ，１０や遮光膜１２が下地層として形成されており、また、図２２に示すように、周辺回路領域（ゲート線駆動回路２２Ｒ，２２Ｌ，プリチャージ及びテスト回路２３，画像信号サンプリング回路２４，及びデータ駆動回路２１）では、画素選択用ＭＯＳＦＥＴの電極配線７ａ，素子相互間の配線１２ｂが下地層として形成されており、更に、端子パッド２６の領域では第１のメタル層からなる下層膜６ａ，第２のメタル層からなる上層膜２６ｂが積み重ね形成されているため、第３の層間絶縁膜１３の成膜直後で

は図２２の点線で示す表面レベル１３ａは画素領域，周辺回路領域及び端子パッド領域で盛り上がっている。かかる表面起伏の大きな第３の層間絶縁膜１３の被研磨面をＣＭＰ法で研磨処理すると、図２２の実線で示す研磨仕上がりレベル１３ｂも必然的に点線で示す表面起伏が反映したものとなる。本願の発明者による鋭意研究によれば、このような研磨処理を施した液晶パネル用基板３１においては、特に、画素領域２０上の第３の層間絶縁膜１３の表面の平坦化が重要であることが判明した。

【００１６】この画素領域２０上の第３の層間絶縁膜１３を平坦化する技術として、特開平９－６８７１８号公報には、中継配線１０等の第１のメタル層と第２のメタル層（遮光膜）１２との間に画素毎の孤立したメタル層のダミーパターンを予め介在させて底上げし、遮光膜１２の全表面の起伏を抑える構造が採用されている。しかし、このような画素毎の底上げのためだけに中間メタル層を成膜すると、層間絶縁膜の成膜工程も追加せざるを得ない。また、研磨前の層間絶縁膜の表面起伏が抑えられてるいと、却ってＣＭＰ処理の初期研磨レートが低くなり、層間絶縁膜１３の表面を鏡面様に平坦化するために必要な研磨時間が長くなり、砥液の消費も増大する。従って、画素領域２０の画素毎にダミーパターンを成膜する構造は、製造プロセス上のデメリットがあり、製造コスト高を招く。

【００１７】

【発明が解決しようとする課題】図２３は第３の層間絶縁膜１３を膜厚約２４０００Åで成膜した後、その画素領域２０の中心部の第３の層間絶縁膜１３の残膜厚が約１２０００ÅになるまでＣＭＰ処理を施した液晶パネル用基板３１における研磨後の第３の層間絶縁膜１３の膜厚分布を示す等膜厚線図である。また、図２４中のプロット×印を連ねるグラフは図２３中のａ－ａ′線に沿うシール左辺縦方向の残膜厚の分布を示し、図２５中のプロット×印を連ねるグラフは図２３中のｂ－ｂ′線に沿う画素中央縦方向の残膜厚の分布を示し、図２６中のプロット×印を連ねるグラフは図２３中のｃ－ｃ′線に沿うシール上辺横方向の残膜厚の分布を示し、図２７中のプロット×印を連ねるグラフは図２３中のｄ－ｄ′線に沿う画素中央横方向の残膜厚の分布を示し、図２８中のプロット×印を連ねるグラフは図２３中のｅ－ｅ′線に沿う画素中央横方向の残膜厚の分布を示す。

【００１８】図２３～図２８から判るように、画素領域２０及びシール領域２７での最大膜厚差は約６１２０Åもあり、画素領域２０及びシール領域２７を含め基板全体に亘る平坦性はまだ不十分なものである。また、端子パッド２６の周囲領域やシール領域２７の上下辺の中央部が過研磨状態となっている一方、シール領域２７の左右辺の中央部が研磨不足状態となっている。

【００１９】図２２に示すように、端子パッド２６の領域ではスポット状孤立高の端子パッド２６が離散的に列状に配されているため、第３の層間絶縁膜１３で覆われた孤立高１３ｃの部分に易研磨性が現れる。従って、端子パッド２６の領域は画素領域２０よりも初期研磨レートが大きくなるため、画素領域２０がまだ充分平坦化されないのに、端子パッド２６の領域が過剰研磨されて下地層（上層膜２６ｂ）が露出してしまう危険性がある。

【００２０】このような端子パッド２６での過剰研磨状態を解消する手段として、予め第３の層間絶縁膜１３を厚く堆積する方法が挙げられる。この方法によれば、端子パッド２６の領域の研磨が速く進行しても、下地層が露出する前にこの領域での第３の層間絶縁膜１３の平坦化がほぼ完了するので、それ以降の研磨レートは初期研磨レートに比べて著しく低下し、画素領域２０の平坦化のために研磨時間を増やしても、下地層の露出を防ぐことができる。

【００２１】しかし、厚い第３の層間絶縁膜１３を形成した場合、接続プラグ１５のためのコンタクトホール１６が却って深くなり、アスペクト比が大きくなるため、接続プラグ１５を構成する高融点金属でコンタクトホール１６を埋め難くくなる。特に、接続プラグ１５は第２の層間絶縁膜１１と遮光膜１５を貫通してから第３の層間絶縁膜１３を貫通して画素電極１４に繋げるための飛び越し層間導電部であり、コンタクトホール１６自身は元々深くなり易い。また画素電極１４間の隙間から入射する光が開口部１２ａを介してＭＯＳＦＥＴ等の素子に極力進入し難くするためには、開口部１２ａをできるだけ小さくする必要上、コンタクトホール１６の孔径も細くせねばならない。このため、必然的にコンタクトホール１６のアスペクト比は大きくなる。それ故、被研磨層の第３の層間絶縁膜１３の薄膜化が強く要請される。しかし、上述したように、端子パッド２６の領域では第３の層間絶縁膜１３のＣＭＰ法による平坦化処理の過研磨が顕在化してしまう。

【００２２】他方、シール領域２７の上下辺の中央部の膜厚は端子パッド２６の領域での過研磨に引きずられて画素領域２０の膜厚に比べ相対的に薄くなっているため、図２６及び図２８に示すように、画素領域２０の上下縁又はシール領域２７の上下辺は中央部が過研磨状態である。また、シール領域２７の左右辺の四隅部付近も端子パッド２６の領域での過研磨に引きずられて膜厚が薄くなり易いが、シール領域２７の左右辺の中央部は研磨前のシール領域２７の平坦性の故に却って初期研磨レートが落ち研磨し難くなっている。このため、図２４に示すように、シール領域２７の左右辺や画素領域２０の左右縁は中央部が研磨不足状態である。このように、画素領域２０の周囲縁やシール領域２７が勾配面を有していると、研磨後の第３の層間絶縁膜１３上に形成される画素電極１４の反射効率の低下や液晶パネル組立の際のセルギャップ調整の困難やシール材の密着性不具合をもたらし、また、接続プラグ１５のコンタクトホール１６

をＣＭＰ処理後に穴明けする場合は、膜厚不均一によりコンタクトホールのエッチング時間の最適化が困難となる。

【００２３】そこで、反射型液晶パネル用基板における遮光膜と画素電極との間に形成される研磨処理を要する層間絶縁膜についての二律背反した上述の問題点に鑑み、本発明の第１の課題は、素子領域が形成された基板の上に層間絶縁膜と導電層を交互に繰り返して成膜した積層膜構造を有する電気光学装置用基板において、成膜工数の追加を招かず、上記の研磨すべき層間絶縁膜も厚膜化せずに、その層間絶縁膜の研磨レートを均一化できる構造を持つ液晶パネル用基板等の電気光学装置用基板を提供することにある。

【００２４】また本発明の第２の課題は、シール領域も画素領域と同様に層間絶縁膜の研磨面が平坦面となり、画素電極の反射効率の向上，セルギャップ調整の容易化，シール材の密着性向上，コンタクトホールのエッチング時間の最適化を実現できる液晶パネル用基板等の電気光学装置用基板を提供することにある。

【００２５】

【課題を解決するための手段】上記第１の課題を解決するため、本発明の講じた第１の手段は、研磨前の層間絶縁膜の成膜表面レベルを少なくとも画素領域内でできるだけ全面均一に平坦化するべく、上記研磨処理の層間絶縁膜の底上げ用のダミーパターンを画素領域内の空き間に作り込むのではなく、既成配線層を援用して画素領域外に略一面的に形成する点にある。即ち、本発明は、各画素に対応するスイッチング素子が基板上に配置される画素領域において、複数の層間絶縁膜と複数の導電層とが交互に積層された積層膜構造を有しており、該複数の導電層のうちの最上層の導電層より下層の少なくとも一層の前記層間絶縁膜が研磨処理で平坦化されて成る電気光学装置用基板であり、前記基板上の非画素領域において形成された少なくとも端子パッドの近傍には、前記研磨処理の層間絶縁膜よりも下層の前記導電層からなる単層又は複層のダミーパターンを有して成ることを特徴とする。ここに、端子パッドとしては、基板縁近傍に配置される入力端子パッドやそれよりも基板内方に配置される中継端子パッドが含まれる。

【００２６】このようなダミーパターンを端子パッドの近傍に配置した構造においては、端子パッドの近傍でもダミーパターン上の研磨の層間絶縁膜の成膜表面レベルが底上げされるため、画素領域での研磨処理の層間絶縁膜の成膜表面レベルと略同等レベルになり、表面レベルが全体に亘り均一化する。このように、被研磨面を均一化すると、ＣＭＰ（化学的機械研磨）等の研磨を施した際、端子パッド領域の近傍・周囲の研磨レートが徒に速くならず、全体的に一様の研磨レートが得られて、研磨処理の層間絶縁膜の研磨面が従前に比し平坦化する。このため、画素領域の平坦化も一層良好となり、対向基板等を用いたセル組立時のセルギャップの制御性を改善できると共に、研磨後の画素領域の層間導電部等のコンタクトホールのエッチング時間を決定し易くなる。

【００２７】このような研磨面の一様平坦化が得られると、端子パッド部の過研磨により下地の端子パッド層の露出が起こり難くなり、また研磨処理に係る層間絶縁膜の薄膜化も実現できる。この薄膜化により、画素領域にある層間導電部のコンタクトホールのアスペクト比を改善できるので、コンタクトホールの細径化により開口部の細径化に結び付けることができる。それ故、遮光性能を改善できる。

【００２８】なお、この層間導電部は、スイッチング素子に電気的に接続する第１の前記導電層と前記研磨処理の層間絶縁膜の上に成膜された上層の前記導電層とを電気的に接続するものであるが、前記ダミーパターンは、第１の導電層からなる第１のダミーパターン、及び第１の導電層と遮光膜等の上層の導電層との中間にある第２の導電層からなる第２のダミーパターンのいずれか又は両者の積み重ねとすることができる。

【００２９】そして、画素領域外の端子パッドの近傍域にも導電層のダミーパターンが敷き詰められていると、このダミーパターンも遮光膜となるため、迷光が画素領域外から基板に作り込んだ素子領域に入り難くなり、光電流を抑制でき、スイッチング素子特性の改善に役立つ。

【００３０】ところで、通常、入力端子パッドと外部配線との接続においては異方性導電膜を熱圧着するようにしているので、ダミーパターン領域を覆う研磨後の比較的薄い前記層間絶縁膜が導電性粒子で傷つけられ、入力端子パッドとショートを引き起こす新たな危惧が生じる。入力端子パッドの近傍に配置されたダミーパターンが引出し配線の領域を除いて四方一面に略連続して形成されて成る場合、このダミーパターンを介して隣接する入力端子パッド間がショートする虞れがある。

【００３１】しかし、本発明においては、入力端子パッドの周囲に配置されたダミーパターンが平面的に細分化された複数の小分けダミーパターンからなるため、成膜直後の研磨処理すべき層間絶縁膜の表面レベルを均一化しながら、隣接の端子パッド間のショートを防止できる。小分けダミーパターンの数を増やす程に、ショート確率はより僅少になる。

【００３２】ここで、相隣り合う入力端子パッドの間は非ダミーパターン領域であることが好ましい。この非ダミーパターン領域には熱圧着時に強い押し付け力が加わるフレキシブルテープ配線の導電線に隣接している。仮にダミーパターンが連続して形成されていると、異方性導電膜中の導電性微粒子によって端子パッドとショートする確率が高く、またダミーパターンとのショートを介して入力端子パッド間のショートを招く危険性もある。非ダミーパターン領域とするのは、このような危険性の

高いショートを確実に防止するためである。

【００３３】この入力端子パッドとその周囲に配置された小分けダミーパターンとの間隔は、配線とその近傍のダミーパターンとの間隔よりも広く設定されてなる。異方性導電膜の導電性粒子による入力端子パッドと小分けダミーパターンとの架橋が起こり難くなり、ショートを極力防止するためである。

【００３４】また、中継端子パッドとその周囲に配置されたダミーパターンとの間隔は、配線とその近傍のダミーパターンとの間隔よりも広く設定されてなる。中継端子パッド上では通常銀ペーストで導通が図られるようになっているが、銀ペーストが中継端子パッドから若干はみ出しても、その近傍のダミーパターンに極力ショートしないようにしている。

【００３５】上記第２の課題を解決するため、本発明の第２の手段は、端子パッドの近傍域に限らず、画素領域の周囲に形成されるシール領域に、前記研磨処理の層間絶縁膜よりも下層の導電層からなる単層又は複層のダミーパターンを有して成ることを特徴とする。シール領域にダミーパターンが敷設されていないと、画素領域の前記研磨処理の層間絶縁膜表面は、特にその周辺部分において勾配面となり易く、この後に形成されるべき上層の導電層の遮光膜の反射効率の低下や、前記研磨処理の層間絶縁膜の膜厚不均一によるホールのエッチング時間最適化の困難を招来する。このような問題を解消するためには、シール領域にダミーパターンを設けると良い。これによって画素領域の周辺に近い領域はシール領域も含め前記研磨処理すべき層間絶縁膜の表面レベルはほぼ均一となるので、研磨処理を施しても画素領域における研磨処理の層間絶縁膜に勾配面や膜厚不均一は生じ難い。

【００３６】しかし、ダミーパターンを設けたシール領域の更に外側にダミーパターンが設けられていないと、研磨処理によってシール領域上の層間絶縁膜が勾配面となってしまう。これは、電気光学装置の組立において、対向基板と貼り合わせる際の基板間ギャップ（セルギャップとも言う）の制御に支障を来たしたり、シール材の密着性に不具合を生じたりする。

【００３７】これを解決するために、シール領域の更に外側の外周領域にも、ダミーパターンを設けることが好ましい。

【００３８】なお、このダミーパターンは、スイッチング素子に電気的に接続する第１の導電層からなる第１のダミーパターン、及び第１の導電層と遮光膜等の前記上層の導電層との中間にある第２の導電層からなる第２のダミーパターンのいずれか又は両者の積み重ねとすることができる。

【００３９】更に、このシール領域及びシール領域の外周領域に設けるダミーパターンは、スイッチング素子の制御配線層と同層で孤立したパターンの上に積み足されて成ることが好ましい。また、必要があれば、端子パッドの近傍域のダミーパターンも、スイッチングの制御配線層と同層で孤立したパターンの上に積み足されて成ることが好ましい。このパターンをも底上げ用の台板として利用すると、前記研磨処理の層間絶縁膜の表面レベルの平坦化を更に微細に調節できる。

【００４０】そしてまた、本発明においては、画素領域の周辺に配置されスイッチング素子に信号を供給する駆動回路の近傍領域には、前記研磨処理の層間絶縁膜よりも下層の導電層からなる単層又は複層のダミーパターンを有して成ることを特徴とする。シール領域と画素領域との中間領域などにも、ダミーパターンを形成することにより、前記研磨処理の層間絶縁膜の平坦化等に役立つ。なお、このダミーパターンは、前記第１の導電層からなる第１のダミーパターン及び前記第２の導電層からなる第２のダミーパターンのいずれか又は両者の積み重ねとすることができる。

【００４１】更に、本発明においては、画素領域の周囲に形成されるシール領域の隅部領域には、該シール領域の辺領域又は当該隅部の周辺領域よりも密度の低い分布であり、前記研磨処理の層間絶縁膜よりも下層の前記導電層からなる単層又は複層のダミーパターンを有して成ることを特徴とする。シール領域の隅部領域内では、シール辺部又は当該隅部の周辺領域のダミーパターンの様な広い連続拡張面（いわゆるベタ）ではなく、複数の小分けダミーパターンの分散的集合となっている。このため、シール四隅部における研磨前の層間絶縁膜の表面は離散的な複数の小分けダミーパターンによる凹凸が反映した面粗さを呈しており、研磨処理を施すと、四隅部を連続拡張面で形成する場合よりも、初期研磨レートが速くなり、四隅部の研磨レート並びにシール領域内側の研磨レートと略平等化する傾向で進行するので、画素領域及びシール領域の残膜厚バラツキが抑制される。

【００４２】また、画素領域の周囲に形成されるシール領域には、その隅部領域を除き、前記研磨処理の層間絶縁膜よりも下層の前記導電層からなる単層又は複層のダミーパターンを有して成る場合、即ち、四隅部において全くダミーパターンがない（パターン密度ゼロ）場合でも、隅部が落ち込みその境界部分が立ち上がっている（角ばっている）ため、研磨初期ではその境界部分が易研磨状態になって勾配面が形成され、除々に画素領域及びシール領域の内方へ勾配面が波及する。このため、画素領域及びシール領域の全体的な平坦化を得ることができる。

【００４３】なお、このようなダミーパターンは、前記第１の導電層からなる第１のダミーパターン及び前記第２の導電層からなる第２のダミーパターンのいずれか又は両者の積み重ねとすることができる。

【００４４】そしてまた、本発明においては、非画素領域に連続拡張面（いわゆるベタ）のダミーパターンを形成するではなく、基板上の非画素領域において前記研磨

処理の層間絶縁膜よりも下層の前記導電層を含む複数の擬似画素凹凸パターンを有して成ることを特徴とする。このような擬似画素凹凸パターンを具える基板では、研磨処理前の層間絶縁膜の画素領域以外の表面にも、画素の表面凹凸模様と略類似の表面凹凸模様が形成されているため、研磨レートが初期から基板のどの部分でも略等しくなり、少なくとも画素領域及びシール領域では高精度の表面平坦性を実現できる。

【００４５】複数の擬似画素凹凸パターンを非画素領域に非規則的に配置するよりも、基板上の２次元方向に繰り返し展開形成し、空間規則性を持たせる方が好ましい。画素領域に画素凹凸パターンがマトリクス状などの空間規則性を有していることに対応させるためである。画素領域及びシール領域での表面平坦性が顕著になる。

【００４６】この擬似画素凹凸パターンは、前記第１の導電層からなる第１のダミーパターン及び前記第２の導電層からなる第２のダミーパターンのいずれか又は両者の積み重ねで構成できるが、層間絶縁膜のパターンをも含ませることにより擬似度合いを一層高めることができる。

【００４７】そして、この擬似画素凹凸パターンとしては、少なくとも擬似ゲート線及び擬似データ線で構成することが好ましい。これらが画素の凹凸の顕著な（代表的）部分であり、また画素領域の凹凸規則性に最も関与するからである。

【００４８】なお、上記の電気光学装置用基板を用いて電気光学装置が組立られるが、このような電気光学装置は各種電子機器の表示部に用いるに適している。例えば、投写型表示装置のライトバルブに好適である

【００４９】

【発明の実施の形態】次に、本発明の各実施形態を添付図面に基づいて説明する。

【００５０】〔実施形態１〕図１は本発明の実施形態１に係る反射型液晶パネルの反射型液晶パネル用基板のレイアウト構成例を示す平面図、図２は図１中のＢ－Ｂ′線に沿って切断した状態を示す切断図である。

【００５１】図１に示す本例の反射型液晶パネル用基板１３１は、従来の液晶パネル用基板を示す図１８及び図１９の基板３１と同様に、図１８に示す画素電極１４がマトリクス状に配置された矩形の画素領域（表示領域）２０と、画素領域２０の左右辺の外側に位置し、ゲート線（走査電極，行電極）を走査するゲート線駆動回路（Ｙドライバ）２２Ｒ，２２Ｌと、画素電極１４の上辺の外側に位置し、データ線（信号電極，列電極）についてのプリチャージ及びテスト回路２３と、画素電極１４の下辺の外側に位置し、データ線に画像データに応じた画像信号を供給する画像信号サンプリング回路２４と、ゲート線駆動回路２２Ｒ，２２Ｌ，プリチャージ及びテスト回路２３並びに画像信号サンプリング回路２４の外側には前述したシール材３６（図１８参照）が位置決めされるシール領域１２７と、下側端に沿って配列されており、異方性導電膜を介してフレキシブルテープ配線に固着接続される複数の入力端子パッド２６と、この端子パッド２６の列とシール領域１２７の下辺との間に位置し、画像信号サンプリング回路２４にサンプリング信号を供給するデータ線駆動回路（Ｘドライバ）２１と、そのデータ線駆動回路２１の両脇に位置し、入力端子パッド２６から液晶交流駆動の振幅中心電圧を図１８に示すガラス基板３５の対向電極３３に給電するための中継端子パッド（いわゆる銀点）２９Ｒ，２９Ｌとから構成されている。ゲート線駆動回路２２Ｒ，２２Ｌとデータ線駆動回路２１は各々シフトレジスタを有し、シフトレジスタでのシフトデータの転送に応じて、走査信号をゲート線に、サンプリング信号を画像信号サンプリング回路２４に各々供給する。信号サンプリング回路２４はサンプリング信号を受けて画像信号をデータ線に供給する。

【００５２】特に、本例では、画素領域２０を取り囲む枠形状（額縁状）のシール領域１２７はハッチングで示すような孤立した連続拡張面（いわゆるベタ）のダミーパターン領域となっている。また、入力端子パッド２６，中継端子パッド２９Ｒ，２９Ｌやデータ線駆動回路２１の周囲もハッチングで示すような連続拡張面のダミーパターン領域となっている。

【００５３】このパネル基板１３１の画素領域２０の平面構造及び断面構造は図２０及び図２１に示す構造と同じである。即ち、図２に示すように、大形サイズ（約２０㎜角）で単結晶シリコンのＰ⁻⁻型半導体基板（Ｎ⁻⁻型半導体基板でも良い）１の表面（主面）側にはＰ型ウェル領域２が形成されており、その上にはフィールド酸化膜（いわゆるＬＯＣＯＳ）３が形成されている。このＰ型ウェル領域２は、例えば画素数７６８×１０２４というような画素がマトリクス状に配置された画素領域２０の共通ウェル領域として形成されており、周辺回路（ゲート線駆動回路２２Ｒ，２２Ｌ，プリチャージ及びテスト回路２３，画像信号サンプリング回路２４及びデータ線駆動回路２１）を構成する素子を作り込む部分のＰ型ウェル領域２′とは分離されている。

【００５４】フィールド酸化膜３の１画素毎の区画領域には２つの開口部が形成されており、一方の開口部の内側中央にゲート絶縁膜４ｂを介して形成されたポリシリコン又はメタルシリサイド等からなるゲート電極４ａと、このゲート電極４ａの両側のＰ型ウェル領域２の表面に形成されたＮ⁺型ソース領域５ａ，Ｎ⁺型ドレイン領域５ｂとはスイッチング素子，即ち画素選択用のＮチャネル型ＭＯＳＦＥＴ（絶縁ゲート型電界効果トランジスタ）を構成している。図２０に示すように、行方向に隣接する複数の画素の各ゲート電極４ａは走査線方向（画素行方向）に延在してゲート線４を構成している。

【００５５】図２では不図示であるが、図２１に示す如く、他方の開口部の内側のＰ型ウェル領域２の表面に形

成された行方向共通のＰ型容量電極領域８と、このＰ型容量電極領域８の上に絶縁膜（誘電膜）９ｂを介して形成されたポリシリコン又はメタルシリサイド等からなる保持電極９ａとは画素選択用ＭＯＳＦＥＴを介して画素電極１４に供給された画像信号を保持するための保持容量（蓄積容量とも言う）Ｃを構成している。

【００５６】ここに、容量電極９ａは画素選択用ＭＯＳＦＥＴのゲート電極４ａを構成するポリシリコン又はメタルシリサイド層の成膜プロセスを援用して形成できる。また容量電極９ａ下の絶縁膜（誘電膜）９ｂもゲート絶縁膜４ｂを構成する絶縁膜成膜プロセスを援用して形成できる。絶縁膜９ｂ，４ｂは熱酸化法で４００～８００Å程度の膜厚である。容量電極９ａ，ゲート電極４ａは、ポリシリコン層を１０００～２０００Å程度の厚さで形成し、その上にＭｏ又はＷのような高融点金属のシリサイド層を１０００～３０００Å程度の厚さに重ねた複層構造である。ソース，ドレイン領域５ａ，５ｂは、上記のゲート電極４ａをマスクとしてその両側の基板表面にＮ型不純物をイオン打ち込みで自己整合的に注入して形成される。

【００５７】Ｐ型容量電極領域８は、例えば、専用のイオン打ち込みと熱処理（ドライブイン）によるドーピング処理で形成でき、ゲート電極形成工程前にイオン注入を施しても良い。つまり、絶縁膜９ｂの形成後にＰウェル２と同型の不純物を注入し、Ｐ型ウェル２の表面はその深部よりも高不純物濃度領域に成し、低抵抗層を形成する。Ｐ型ウェル２の好ましい不純物濃度は1×10^{17} cm^3 以下で、1×10^{16}～5×10^{16}程度が望ましい。ソース，ドレイン領域５ａ，５ｂの好ましい表面不純物濃度は1×10^{20}～$3\times10^{20}cm^3$ 、Ｐ型容量電極領域８の好ましい表面不純物濃度は1×10^{18}～5×10^{19} cm^3 であるが、保持容量Ｃを構成する絶縁膜９ｂの信頼性及び耐圧の観点からは、1×10^{18}～$1\times10^{19}cm^3$ が望ましい。

【００５８】ゲート電極４ａ及び容量電極９ａの上には第１の層間絶縁膜６が形成され、この絶縁膜６上にはアルミニウムを主体とする第１の導電層（以下，第１のメタル層と言う）が形成されている。第１のメタル層には、列方向に延在するデータ線７（図２０参照），データ線７から櫛歯状に突出してコクタクトホール６ａを介してソース領域４ｂに導電接触するソース電極配線７ａ，コクタクトホール６ｂを介してドレイン領域５ｂに導電接触すると共にコクタクトホール６ｃを介して容量電極９ａに導電接触する中継配線１０とが含まれる。

【００５９】ここに、第１の層間絶縁膜６は、例えばＨＴＯ膜（高温ＣＶＤ法により形成される酸化シリコン膜）を１０００Å程度堆積した上に、ＢＰＳＧ（ボロン及びリンを含むシリケートガラス膜）を８０００～１００００Å程度の厚さで堆積して形成される。ソース電極配線７ａ及び中継配線１０を構成する第１のメタル層は、例えば下層からＴｉ／ＴｉＮ／Ａｌ／ＴｉＮで積層された４層構造とされる。

【００６０】最下層のＴｉは膜厚が１００～６００Å程度、２層目のＴｉＮ層は１０００Å程度、３層目のＡｌ層は４０００～１００００Å程度、最上層のＴｉＮ層は３００～６００Å程度とされる。

【００６１】この第１のメタル層の上には第２の層間絶縁膜１１が形成され、この第２の層間絶縁膜１１上にはアルミニウムを主体とする第２の導電層（以下、第２のメタル層と言う）が形成されている。この第２のメタル層は画素領域２０の大部分を覆い、隣接する画素電極１４の間隔部を遮光する遮光膜１２が含まれる。なお、この遮光膜１２を構成する第２のメタル層は、画素領域２０の周囲に形成される周辺回路（ゲート線駆動回路２２Ｒ，２２Ｌ，プリチャージ及びテスト回路２３，画像信号サンプリング回路２４，及びデータ線駆動回路２１）において素子間の接続用配線１２ｂ（図２参照）としても用いられる。

【００６２】ここに、第２の層間絶縁膜１１は、例えばＴＥＯＳ（テトラエチルオルソシリケート）を材料としプラズマＣＶＤ法により形成される酸化シリコン膜（以下、ＴＥＯＳ膜と称する）を３０００～６０００Å程度堆積した上に、ＳＯＧ膜（スピン・オン・ガラス膜）を堆積し、それをエッチバックで削ってから更にその上に第２のＴＥＯＳ膜を２０００～５０００Å程度の厚さに堆積して形成される。

【００６３】遮光膜１２等を構成する第２のメタル層は、第１のメタル層と同様にしても良く、例えば下層からＴｉ／ＴｉＮ／Ａｌ／ＴｉＮで積層された４層構造とされる。

【００６４】最下層のＴｉは膜厚が１００～６００Å程度、２層目のＴｉＮ層は１０００Å程度、３層目のＡｌ層は４０００～１００００Å程度、最上層のＴｉＮ層は３００～６００Å程度とされる。

【００６５】遮光膜１２の中継配線１０に対応する位置にはプラグ貫通用開口部１２ａが開けられている。遮光膜１２の上には第３の層間絶縁膜１３が形成され、この第３の層間絶縁膜１３の上に略１画素に対応した矩形状の反射電極としての画素電極１４が形成されている。ここに、第３の層間絶縁膜１３も、第２の層間絶縁膜１１と同様にしても良く、ＴＥＯＳ膜を３０００～６０００Å程度堆積した上に、ＳＯＧ膜を堆積し、それをエッチバックで削ってから更にその上に第２のＴＥＯＳ膜を１６０００～２４０００Å程度の厚さに堆積して形成される。或いは、ＴＥＯＳ膜の間にＳＯＧ膜を堆積せず、ＴＥＯＳ膜のみで第３の層間絶縁膜を構成することも可能である。このときの膜厚は１６０００～２４０００Å程度が好ましい。また、ＴＥＯＳ膜の下に窒化シリコン膜を形成したり、ＴＥＯＳ膜の上に窒化シリコン膜を形成したりすることにより、耐湿性を向上させた構成にして

も良い。なお、窒化シリコン膜が上層となる場合はこの窒化シリコン膜を堆積する前にＴＥＯＳ膜をＣＭＰ法等により平坦化するか、窒化シリコン膜そのものをＣＭＰ法等により平坦化することになる。

【００６６】遮光膜１２の開口部１２ａに対応してその内側に位置するように、第３，第２の層間絶縁膜１３，１１を貫通するコンタクトホール１６が設けられている。このコンタクトホール１６内にはタングステン等の高融点金属をＣＶＤ法により埋め込んだ後、第３の層間絶縁膜１３の上に堆積した高融点金属層と第３の層間絶縁膜１３の表面側をＣＭＰ（化学的機械研磨）法で削り込んで鏡面様に平坦化する。このときの層間絶縁膜１３の残りの膜厚は、最も薄い部分で約４０００～１０００Åとなるように研磨量を調整する。

【００６７】次いで、例えば低温スパッタ法によりアルミニウム層を３００～５０００Å程度の厚さに成膜し、パターニングにより一辺が１５～２０μｍ程度の矩形状の画素電極１４を形成する。高融点金属の接続プラグ（層間導電部）１５は、遮光膜１２のメタル層１層分を飛び越し中継配線１０と画素電極１４とを導通させている。なお、接続プラグ１５の形成方法としては、ＣＭＰ法で第３の層間絶縁膜１３を平坦化した後、コンタクトホールを開口し、その中にタングステン等の高融点金属を埋め込む方法もある。また、第２のメタル層１２の開口部１２ａを大きくし、この開口部１２ａ内に第２のメタル層１２からなる第２の中継配線を例えば矩形状に形成し、第１の中継配線１０とこの第２の中継配線を接続し、第２の中継配線と画素電極１４とを接続プラグ１５を介して接続するようにしても良い。そして、画素電極１４の上には厚さ５００～２０００Å程度の酸化シリコン等のパッシベーション膜１７が全面的に形成されている。なお、パッシベーション膜１７上には、液晶パネルを構成する際に配向膜が全面に形成され、ラビング処理が施される。本例では、画素電極１４が第３の導電層（以下、第３のメタル層と言う）により形成されるが、メタル層をより多層化できるプロセスで基板形成する場合は、より上層で形成しても良い。いずれにしても、画素電極１４は複数のメタル層の最上層で形成される。

【００６８】なお、画素領域２０を覆うパッシベーション膜１７としては上述のように酸化シリコン膜が用いられるが、周辺回路領域，シール領域，スクライブ部では２０００～１００００Å程度の厚さの窒化シリコン膜が用いられる。パッシベーション膜１７の上に誘電体ミラー膜を成膜しても良い。

【００６９】図１に示すように、矩形の半導体基板１の大部分を占める画素領域２０の周りには枠状にシール領域１２７が取り囲んでいる。このシール領域１２７は、画素領域２０と液晶が封入されない非画素領域（周辺回路領域，端子パッド領域，スクライブ領域）との境界領域であるが、本例ではシール領域１２７内に周辺回路の一部（ゲート線駆動回路２２Ｒ，２２Ｌ，プリチャージ及びテスト回路２３，画像信号サンプリング回路２４）が含まれており、データ線駆動回路２１のみがシール領域１２７の外側に配置されている。なお、データ線駆動回路２１をシール領域１２７の内側に配置しても良いことは言う迄もない。

【００７０】そして、本例のシール領域１２７の断面構造は、図２に示す如く、フィールド酸化膜３上にゲート電極４ａとは孤立したポリシリコン又はメタルシリサイド等から成る連続拡張面のパターン１２７ａと、第１のメタル層からなる孤立した連続拡張面の下層ダミーパターンＡと、第２のメタル層からなる孤立した連続拡張面の上層ダミーパターンＢとが含まれている。パターン１２７ａはゲート電極４ａの形成プロセスを援用して形成できる。またダミーパターンＡ，Ｂも第１のメタル層と第２のメタル層でのプロセス援用で形成できる。これらパターン１２７ａ，ダミーパターンＡ，Ｂの層厚の分だけ、第３の層間絶縁膜１３の成膜直後ではその表面レベルが一様に底上げされており、画素領域や周辺回路領域の表面レベルに略等しくなっている。

【００７１】シール領域１２７の外側に配されたデータ線駆動回路２１の周囲は勿論のこと、図４～図６及び図９のハッチングで示す如く、中継端子パッド２９Ｒ，２９Ｌや入力端子パッド２６の領域の周囲は配線領域を除いて電気的に浮遊又は電源電圧にクランプされたダミーパターン領域となっている。即ち、本例の入力端子パッド２６も第１のメタル層からなる下層２６ａと第２のメタル層からなる上層２６ｂとを積み重ねた構造となっているが、ダミーパターン領域の断面構造においては、フィールド酸化膜３上の第１の層間絶縁膜６上に形成された第１のメタル層からなる孤立した連続拡張面の下層ダミーパターンＡと、第２の層間絶縁膜１１上に形成された第２のメタル層からなる孤立した連続拡張面の上層ダミーパターンＢとが含まれている。これらのダミーパターンＡ，Ｂもメタル層のプロセス援用で形成できる。そして、これらダミーパターンＡ，Ｂの層厚の分だけ、第３の層間絶縁膜１３の成膜直後ではその表面レベルが積み足されており、その積み足し効果が近傍領域へ反映するため、入力端子パッド２６の真上部分のレベルは、画素領域や周辺回路領域の表面レベルと略等しくなっている。

【００７２】また、図４及び図５に示す如く、シール領域１２７下辺とデータ線駆動回路２１との間の挟間領域Ｘにおいても、データ線駆動回路２１から延び出た複数の配線L_{OUT}間に孤立縦長の配線間ダミーパターンＭが敷き詰められている。この配線間ダミーパターンＭもメタル層を援用して形成される。

【００７３】しかし、入力端子パッド２６の形成法は、下層２６ａの上の第２の層間絶縁膜１１に開けた大きな開口に上層２６ｂを埋め込むものであるから、上層２６

bに大きな中央窪みが形成されるため、その真上の第３の層間絶縁膜１３にも窪みが必然的に形成されてしまう。第３の層間絶縁膜１３の成膜において前述したようにＳＯＧ膜の形成が含まれる場合は、上層２６ｂの窪みをある程度浅くできる。

【００７４】ただ、入力端子パッド２６の占有面積は配線電極のコンタクトホールに比し大規模であるため、ＳＯＧ膜の形成工程の追加だけでは、端子パッド２６真上の第３の層間絶縁膜１３の窪みを充分解消できない。

【００７５】図３は入力端子パッドの別の構造を示す断面図である。図３においては、下層２６ａの上に複数の細径のコンタクトホールを開けてから、上層２６ｂ′を埋め込んで端子パッド２６′が形成される。かかる構造では、コンタクトホール内への上層２６ｂ′の材料の落ち込み量が少なくなり、且つ微細な窪みが分散するため、上層２６ｂ′表面は平坦化される。このため、その上に第３の層間絶縁膜１３を成膜した表面には窪みが反映し難く、平坦化し易い。

【００７６】このように、本例では画素領域や周辺回路領域の外部の殆どの領域において、パターン密度が１００％に近づくように、連続拡張面のダミーパターン領域（ダミーパターンＡ，Ｂ）が積み重ね形成されているため、第３の層間絶縁膜１３の成膜直後でも、その表面レベルが基板全面に亘って略一様レベルになる。それ故、この後、ＣＭＰ研磨処理を施すと、第３の層間絶縁膜１３の研磨面は図２又は図３の実線で示すレベルになる。特に、入力端子パッド２６，２６′の領域では研磨前の第３の層間絶縁膜１３の表面が孤立高とはなっていないので、その領域では初期研磨レートが速すぎず、入力端子パッド２６，２６′が露出し難く、研磨レートが均一化する。このため、ＣＭＰ研磨処理時間、即ち、研磨量を従前量（約４０００Å）よりも増やすことが可能となる。このように研磨レートを均一化できる利益は、結局、研磨後の第３の層間絶縁膜１３の膜厚を薄くできることをもたらす。そして、画素領域２０の遮光膜１２の開口部１２ａに開けたコンタクトホール１６のアスペクト比を改善でき、接続プラグ１５の細径化に寄与するので、開口部１２ａの開口面積を縮小でき、遮光性能を高めることができる。また、研磨量を増やすことができる利益は、第３の層間絶縁膜１３がＴＥＯＳ膜のみからなる場合に生じる開口部１２ａの段差が深くても、ＳＯＧ膜を成膜せずに、ＣＭＰ研磨で段差を緩和できる利益に繋がる。故に、第３の層間絶縁膜１３の成膜プロセスを簡略化でき、生産性の向上に資する。

【００７７】本例のダミーパターン領域の平面レイアウトは、図１のハッチングで示すように、シール領域１２７の外側のうちデータ線駆動回路２１，信号配線，電源配線，入力端子パッド２６，中継端子パッド２９Ｒ．２９Ｌを除いて余すことなく略全面に敷き詰められている。データ線駆動回路（シフトレジスタとその出力に基づきサンプリング信号を生成する論理回路とから成る）２１とシール領域１２７との挟間領域Ｘには、図４又は図５に示すように、配線L_{OUT} 間に形成された孤立縦長の配線間ダミーパターンＭと基板の左右端側のダミーパターンN_R，N_Lとが敷き詰められている。配線L_{OUT}と配線間ダミーパターンＭとの間隔は５μｍ程度である。データ線駆動回路（シフトレジスタ及び論理回路）２１から画像信号サンプリング回路２４へはサンプリング信号を出力する出力配線L_{OUT} が延び出ているため、配線間ダミーパターンＭが規則的に敷き詰められている。また、図６に示すように、入力端子パッド２６の領域から基板の内方へ向かう配線は、データ線駆動回路２１に入力する配線（ＤＸＩＮ（データ信号），電源V_{ddx}，V_{SSX}，クロック信号，反転クロック信号等）ＬＩＮと、ゲート線駆動回路２２Ｒ，２２Ｌ，プリチャージ及びテスト回路２３に入力する配線（ＤＹＩＮ（データ信号），電源V_{ddy}，V_{SSY}，クロック信号，反転クロック信号等）とに大別できるため、入力端子パッド２６から一旦列方向（図示縦方向）に引き出された各配線Ｌは中途の行方向配線領域（図示横方向）Ｗでデータ線駆動回路２１に入力すべき配線L_{IN}とそれ以外の配線とに行く手が別れる。このため、入力端子パッド２６の領域とデータ線駆動回路２１との挟間領域Ｙには、入力端子パッド２６及びそこからの入力配線の間に形成された孤立矩形の複数の小分けダミーパターンS_1～S_3と、データ線駆動回路２１に入力する配線L_{IN}間に形成された孤立矩形の配線間ダミーパターンＴとが敷き詰められている。なお、図６では入力端子パッド２６はその数を減らして図示されている。

【００７８】入力端子パッド２６の平面形状は、その略全体を占める矩形状の導電接触部２６１とそこから左右いずれの側に寄せて基板内方（列方向）へ細幅状に張り出した配線引出し部２６２とから成る。基板の左右中央線から右側に位置する入力端子パッド２６の配線引出し部２６２は導電接触部２６１の左側に寄せて位置しており、基板の左右中央線から左側に位置する入力端子パッド２６の配線引出し部２６２は導電接触部２６１の右側に寄せて位置している。配線引出し部２６２間には孤立横長の小分けダミーパターンS_2が配置されている。更に、配線引出し部２６２の先部間とそこから引き出された配線Ｌ間には孤立矩形の小分けダミーパターンS_3が跨がって形成されている。そしてまた、入力端子パッド２６の基板縁には孤立矩形の小分けダミーパターンS_1が配置されている。

【００７９】前述した基板の左右端側のダミーパターンN_R，N_Lは入力端子パッド２６の位置まで及んで形成されており、左右の最外側の入力端子パッド２６の配線引出し部２６２との間の空き領域には孤立した小分けダミーパターンS_2′が配置されている。また、ダミーパターンN_R，N_Lの先端は入力端子パッド２６の先端に

揃っているが、ダミーパターンN_R，N_Lの先端側の基板縁隅部には孤立した小分けダミーパターンS_0が配置されている。なお、小分けダミーパターンの平面形状は、矩形（正方形，長方形）に限らず、種々の形状（三角形，多角形，曲線形など）を選択できる。例えば、六角形（正六角形）状の小分けダミーパターンを蜂の巣状に敷き詰めて配置しても良い。

【００８０】複数の入力端子パッド２６は図１８に示す如く異方性導電膜（ＡＣＦ）３８を介してフレキシブルテープ配線３９に熱圧着で接続される。図６の破線は異方性導電膜３８の占める領域の縁を示す。フレキシブルテープ配線３９は、図７及び図８に示す如く、絶縁性のフレキシブルテープ３９ａと、この上に被着された複数本のストライプ状の導電線３９ｂとからなる。このフレキシブルテープ３９ａの端部と入力端子パッド２６の列との間には異方性導電膜３８が挟まれている。

【００８１】異方性導電膜３８は粒径５～１０μｍ程度の導電性粒子３８ａと接着用絶縁樹脂材３８ｂとからなる。その膜厚が２～１０μｍ程度にまで押し潰されるまでフレキシブルテープ３９ａを圧着する。端子パッド２６とフレキシブルテープ配線３９の導電線３９ｂとは押し潰されて離散的に分布する導電性粒子３８ａを介して導電接続するため、異方性導電膜３８はその厚み方向にのみ導電性を有している。なお、図７及び図８でも入力端子パッド２６はその数を減らして図示されている。

【００８２】入力端子パッド２６の周囲にダミーパターン領域（ダミーパターンＡ，Ｂ）を積み足すと、前述したように入力端子パッド２６上の成膜直後の第３の層間絶縁膜１３の表面レベルが孤立高ではなく画素領域２０のそれと略同等になるので、研磨工程では入力端子パッド２６の領域でも初期研磨レートが下がり、入力端子パッド２６自身の研磨を防止できると共に、第３の層間絶縁膜１３の薄膜化を実現できる。ここで、仮に各入力端子パッド２６の周囲にダミーパターン領域が連続一面に形成されていると、異方性導電膜３８を熱圧着する場合、導電性微粒子３８ａとダミーパターンを介して入力端子パッド２６間がショートする虞れがある。

【００８３】しかし、本例では、入力端子パッド２６間にはダミーパターンを設けず、非ダミーパターン領域Ｅとなっており、入力端子パッド２６の周囲は小分けダミーパターンS_1～S_3で敷き詰められている。このため、入力端子パッド２６間のショートを防止できる。入力端子パッド２６と小分けダミーパターンS_0～S_3との間隔や、小分けダミーパターンS_0～S_3間の間隔は、配線ＬとダミーパターンS_4との間隔（約５μｍ）よりも広く設定されている。異方性導電膜３８を介したショートを防止するためである。

【００８４】なお、入力端子パッド２６の領域において成膜直後の第３の層間絶縁膜１３の孤立高を更に低減するため、入力端子パッド２６間にもダミーパターンを形成しても良いが、入力端子パッド２６間のショートを防止すためには、入力端子パッド２６間に形成されるダミーパターンも小分けダミーパターンとする。小分けダミーパターンの小分け数を増やす程に、ショート確率はより僅少になる。ただ、小分け数が増せば増すほど、ダミーパターン領域上の成膜直後の第３の層間絶縁膜１３の表面に起伏が顕在化するため、適度の数を選定することが好ましい。小分けダミーパターンの平面形状は、矩形（正方形，長方形）に限らず、種々の形状（三角形，多角形，曲線形など）を選択できる。例えば、六角形（正六角形）状の小分けダミーパターンを蜂の巣状に敷き詰めて配置しても良い。

【００８５】図９は中継端子パッド２９Ｒの周辺を示す部分平面図である。中継端子パッド２９Ｒ（２９Ｌ）は、データ線駆動回路２１の脇で最外側の端子パッド２６からの配線（液晶の交流駆動における液晶印加電圧の極性反転の基準となる電位の供給配線）Ｌに繋がった矩形パッドであり、銀ペーストを着けてガラス基板３５の対向電極３３に導電接続される。この中継端子パッド２９Ｒ（２９Ｌ）の周囲にはダミーパターンN_R，N_Lが形成されている。このため、中継端子パッド２９Ｒ（２９Ｌ）においても端子パッド２６と同様に、成膜直後の第３の層間絶縁膜１３の表面レベルを均一化できる。」本例では中継端子パッド２９ＲとダミーパターンN_Rとの間隔を例えば７０μｍに設定してあり、銀ペーストを付着させた際のはみ出しが多少起こっても、ショートし難い間隔に設定してある。即ち、中継端子パッド２９ＲとダミーパターンN_Rとの間隔は、配線とその近傍のダミーパターンとの間隔より広く設定されている。なお、中継端子パッド２９Ｒ周囲のダミーパターンも小分けダミーパターンとしても良い。

【００８６】図１０は、実施形態１において第３の層間絶縁膜１３を膜厚約２４０００Åで成膜した後、その画素領域２０の中心部の第３の層間絶縁膜１３の残膜厚が約１２０００ÅになるまでＣＭＰ処理を施した液晶パネル用基板１３１における研磨後の第３の層間絶縁膜１３の膜厚分布を示す等膜厚線図である。また、図２４中のプロット△印を連ねるグラフは図１０中のａ－ａ′線に沿うシール左辺縦方向の残膜厚の分布を示し、図２５中のプロット△印を連ねるグラフは図１０中のｂ－ｂ′線に沿う画素中央縦方向の残膜厚の分布を示し、図２６中のプロット△印を連ねるグラフは図１０中のｃ－ｃ′線に沿うシール上辺横方向の残膜厚の分布を示し、図２７中のプロット△印を連ねるグラフは図１０中のｄ－ｄ′線に沿う画素中央横方向の残膜厚の分布を示し、図２８中のプロット△印を連ねるグラフは図１０中のｅ－ｅ′線に沿う画素中央横方向の残膜厚の分布を示す。

【００８７】これらの図から判るように、画素領域２０及びシール領域１２７での最大膜厚差は約２７２０Åであり、等厚線の間隔（膜厚差１０００Å）が図２３のそ

れに比し相当広くなっている。画素領域２０の平坦性が２倍以上も改善されている。

【００８８】基板（チップ）全体での最大膜厚差は約２９１０Åに抑制されている。シール領域１２７の上辺の中央部が低い勾配は略１／２以下に減少し、シール領域１２７の下辺の中央部が低い勾配は略１／４以下にも減少している。更に、シール領域１２７の左右辺は上隅部が最も薄く、中央部が高い勾配が解消されており、勾配は略１／４以下にも減少している。このような顕著な改善は、画素領域２０や周辺回路領域の外部の殆どの領域において、連続拡張面（ベタ）のダミーパターン領域（ダミーパターンＡ，Ｂ）が敷き詰められているためである。

【００８９】しかし、画素領域２０の最大膜厚差を１０００Å以下に抑えることが望まれる。画素領域２０の膜厚分布には画素中央縦線が膜厚の谷線となっており、入力端子パッド２６の領域における中央部の膜厚が最大膜厚（約１４５００Å）となっている。これは、図２３の従来例とは逆に入力端子パッド２６の領域が研磨不足になったものと考えられる。

【００９０】〔実施形態２〕図１１は本発明の実施形態２に係る反射型液晶パネル用基板においてシール領域の四隅部の近辺を示す部分平面図、図１２は図１１中のＣ－Ｃ′線に沿って切断した状態を示す断面図である。なお、図１１において、散点模様の領域は第１のメタル層を、一様斜線のハッチング領域は第２のメタル層をそれぞれ表し、第３のメタル層は不図示である。また、以下に説明する内容以外の構成は、実施形態１に係る反射型液晶パネル用基板と同様である。

【００９１】本例の反射型液晶パネル用基板２３１も実施形態１の反射型液晶パネル用基板１３１と略同様の構成を有しており、画素領域２０を取り囲むシール領域１２７は孤立した連続拡張面（いわゆるベタ）のダミーパターン領域（第１のメタル層のダミーパターンＡと第２のメタル層のダミーパターンＢ）となっていると共に、入力端子パッド２６，中継端子パッド２９Ｒ，２９Ｌやデータ線駆動回路２１の周囲も連続拡張面のダミーパターン領域（第１のメタル層のダミーパターンＡと第２のメタル層のダミーパターンＢ）となっている。実施形態１のダミーパターン形成態様と異なる点は、シール領域１２７のシール四隅部１２７Ｃの矩形領域内では、第１のメタル層のダミーパターンは、シール辺部の配線Ｌ$_{OUT}$間に敷き詰めたダミーパターンＡの様な広い連続拡張面（いわゆるベタ）ではなく、複数の小分けダミーパターンａの分散的集合となっている。即ち、矩形又は短冊状の面積の異なる複数の小分けダミーパターンａが間隔をおいてそれぞれ縦横方向に揃えて分散的に敷き詰められており、５０％以下のパターン密度になっている。複数の小分けダミーパターンａの面積はそれぞれ異なるが、入力端子パッド２６の面積よりも皆小さい。シール四隅部１２７Ｃにおける第２のメタル層のダミーパターンＢ′は矩形状の連続拡張面である。このため、シール四隅部１２７Ｃにおける研磨前の第３の層間絶縁膜１３の表面は図１２の点線で示すように離散的な複数の小分けダミーパターンａによる凹凸が反映した面粗さを呈している。

【００９２】シール四隅部１２７Ｃに密度の低い分布の小分けダミーパターンａを設けた基板において、第３の層間絶縁膜１３の表面をＣＭＰ処理すると、シール領域１２７の辺部の平坦に近い起伏に比し四隅部１２７Ｃの初期研磨レートが速くなるため、これに引きずられる形で四隅部１２７ａの４部位で囲まれたシール領域１２７及びその内側領域の研磨レートが略平等化する傾向で進行するので、画素領域２０及びシール領域１２７の残膜厚バラツキが抑制される。特に、４部位のシール四隅部１２７ａのうちでも、シール領域１２７の下辺の左右隅部に予め粗さ度を付与した意義は大きいと言える。

【００９３】ここで、シール四隅部１２７Ｃにおける複数の小分けダミーパターンａの島状面積を略等しくして、均等分散的ないしランダムに分布していると仮定し、パターン密度（単位面積においてダミーパターンの面積の総和が占める割合）を低くすることは、ダミーパターンａ間が空くので小分けダミーパターンａが粗く分布する。このため、第３の層間絶縁膜１３の初期研磨レートはシール四隅部１２７Ｃの周辺に比べて速くなり、シール四隅部１２７Ｃの境界部分が速く勾配面となり易く、この勾配面は除々に研磨されて内方へ波及する。パターン密度が同じ場合、小分けダミーパターンａの数を減らし、面積を大きくすると、孤立高の傾向が強くなり、初期研磨レートは速くなる。このため、シール四隅部１２７Ｃの境界部分は速く勾配面となり易く、上記と同等に、この勾配面は除々に研磨されて内方へ波及する。本例では、シール四隅部１２７Ｃの初期研磨レートをその周囲よりも高めるダミーパターン分布を採用することにより、４部位のシール四隅部１２７Ｃで囲まれたシール領域１２７の辺部や画素領域２０での残膜厚を基準たるシール四隅部１２７Ｃの残膜厚に引きずられて合わせ易くなる。シール領域１２７及び画素領域２０の平坦制御化が実現されている。

【００９４】図１１に示すように、シール四隅部１２７Ｃでは、シール辺の左右辺には縦方向に離散配列した複数の短冊状小分けダミーパターンａが隣接しており、シール辺の上下辺には横方向に離散配列した複数の短冊状小分けダミーパターンａが隣接している。縦方向の短冊状小分けダミーパターンａの存在はその長辺部分（縦方向部分）で初期研磨レートが最も速いのでシール上下辺方向の平坦化に寄与し、また横方向の短冊状小分けダミーパターンａの存在はその長辺部分（横方向部分）で初期研磨レートが最も速いのでシール左右辺方向の平坦化に寄与するものと考えられる。縦方向の短冊状小分けダ

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ミーパターンａがシール上下辺に隣接すると共に横方向の短冊状小分けダミーパターンａがシール左右辺に隣接しているのではなく、本例では、縦方向の短冊状小分けダミーパターンａがシール左右辺に隣接しており、また横方向の短冊状小分けダミーパターンａがシール上下辺に隣接しているため、シール四隅部１２７Ｃ内での縦方向と横方向の初期研磨レートが交錯し、結果的にこの部分での初期研磨レートが速くなるものと考えられる。なお、小分けダミーパターンａの形状，配列及びパターン密度を種々変えることにより、シール領域１２７及びその内側領域の平坦化が一層改善できるものと考えられる。

【００９５】また、シール四隅部１２７Ｃにおいて全くダミーパターンがない（パターン密度ゼロ）場合でも、隅部がその周囲に比べ落ち込んで窪み状になり、その境界部分が立ち上がっているため、研磨初期ではその境界部分が易研磨状態になって勾配面が形成され、除々に画素領域及びシール領域の内方へその勾配面が波及する。このため、画素領域２０及びシール領域１２７の全体的な平坦化を得ることができる。

【００９６】図１３は、実施形態２において第３の層間絶縁膜１３を膜厚約２４０００Åで成膜した後、その画素領域２０の中心部の第３の層間絶縁膜１３の残膜厚が約１２０００ÅになるまでＣＭＰ処理を施した液晶パネル用基板２３１における研磨後の第３の層間絶縁膜１３の膜厚分布を示す等膜厚線図である。また、図２４中のプロット□印を連ねるグラフは図１３中のａ－ａ′線に沿うシール左辺縦方向の残膜厚の分布を示し、図２５中のプロット□印を連ねるグラフは図１３中のｂ－ｂ′線に沿う画素中央縦方向の残膜厚の分布を示し、図２６中のプロット□印を連ねるグラフは図１３中のｃ－ｃ′線に沿うシール上辺横方向の残膜厚の分布を示し、図２７中のプロット□印を連ねるグラフは図１３中のｄ－ｄ′線に沿う画素中央横方向の残膜厚の分布を示し、図２８中のプロット□印を連ねるグラフは図１３中のｅ－ｅ′線に沿う画素中央横方向の残膜厚の分布を示す。

【００９７】これらの図から判るように、画素領域２０及びシール領域１２７での最大膜厚差は約１３８０Åであり、等厚線の間隔（膜厚差１０００Å）が図１０のそれに比し更に間延びしている。実施形態１に比し、本例では画素領域２０の平坦性が２倍以上も改善されている。基板（チップ）全体での最大膜厚差は約２５００Åであるが、これは入力端子パッド２６の領域でダミーパターンが連続拡張面であるため、研磨不足でなおも膜厚が厚いからである。シール領域１２７の上辺の中央部が低い勾配も実施形態１に比し略１／２以下に減少しいる。また、シール領域１２７の左右辺は略平坦になっている。これはシール領域１２７の下辺の左右隅部のダミーパターンａのパターン密度を低くしたことで、研磨し易くなったからである。

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【００９８】しかし、図１３から理解できるように、シール領域１２７の下辺の左右隅部の周辺の膜厚はまだ厚く、画素領域２０及びシール領域１２７での最大膜厚差は１００Å以下とはなっていない。四隅部１２７Ｃのダミーパターンａを全く無くした（パターン密度ゼロ）場合は、画素領域２０内側はより平坦化するものの、四隅部１２７Ｃの境界部分は急勾配となるおそれがある。下辺の左右隅部１２７Ｃから左右辺の上方へ向かうにつれパターン密度が漸減するダミーパターンａを形成し、又は、下辺の左右隅部１２７Ｃから下辺の中央へ向かうにつれパターン密度が漸減するダミーパターンａを形成しても良い。かかる場合、画素領域２０及びシール領域１２７の両領域の更なる平坦化を実現できる。

【００９９】〔実施形態３〕図１４は本発明の実施形態３に係る反射型液晶パネル用基板においてシール領域の四隅部の近辺を示す部分平面図、図１５は図１４中のＣ－Ｃ′線に沿って切断した状態を示す断面図である。なお、図１４において、散点模様の領域は第１のメタル層を、一様斜線のハッチング領域は第２のメタル層をそれぞれ表し、第３のメタル層は不図示である。また、以下に説明する内容以外の構成は実施形態１に係る反射型液晶パネル用基板と同様である。

【０１００】本例の反射型液晶パネル用基板３３１は、画素領域２０を取り囲むシール領域２２７及びその外側領域においてマトリクス状（２次元周期状）に敷き詰められたダミーパターンとしての擬似画素凹凸パターンＰを有している。この擬似画素凹凸パターンＰは、データ線駆動回路２１や中継端子パッド２９Ｒ，２９Ｌの周囲や入力端子パッド２６の周囲にも余すことなく縦横方向へ展開拡張して形成されている。この擬似画素凹凸パターンＰは画素領域２０を構成する画素の構成要素のボリュウムを模して第３の層間絶縁膜１３の表面に画素表面と類似の凹凸形状模様を得るためのものである。

【０１０１】本例では、擬似画素凹凸パターンＰの構成要素として、画素の最下層配線のゲート線４に見立てた略同線幅の第１のメタル層の擬似ゲート線4_pと、画素の第１のメタル層のデータ線７，ソース電極配線７ａ及び中継配線１０に見立てた略同線幅の第１のメタル層の擬似データ線7_p，擬似ソース電極配線$7a_p$及び擬似中継配線10_pと、画素部分の第２のメタル層の遮光膜１２に見立てた連続拡張面（いわゆるベタ）の第２のメタル層の擬似遮光膜12_pとが存在する。各画素では最下層配線及び第１のメタル層からなるパターン密度は約２５％であるため、擬似画素凹凸パターンＰでの第１のメタル層及び第２のメタル層からなるパターン密度もそれに略合わせてある。

【０１０２】上下のシール領域（辺部）２３７や挟間領域Ｘ′においては、データ線駆動回路２１から画素信号サンプリング回路２４へ第１のメタル層の信号配線ＬOUT がそのまま擬似データ線7_pとして利用されてい

る。このため、第１のメタル層の擬似ゲート線４$_p$′や擬似ソース電極配線７a_p′は擬似データ線７$_p$とは接続されていない。

【０１０３】擬似画素凹凸パターンＰが基板の縦横２次元方向に繰り返し展開されて形成されているが、本例では擬似画素凹凸パターンＰの行列は画素領域２０の行列とは若干食い違っている。データ線駆動回路２１，画素信号サンプリング回路２４，及びゲート線駆動回路２２Ｒ，２２Ｌ等の周辺回路領域の素子レイアウトや信号配線L_{OUT}のレイアウトを設計変更することで、擬似画素凹凸パターンＰの行列と画素領域２０の行列とを揃えることができる。

【０１０４】このような擬似画素凹凸パターンＰを具える基板３３１では、ＣＭＰ処理前の第３の層間絶縁膜１３の画素領域２０以外の表面にも、画素の表面凹凸模様と殆ど類似の表面凹凸模様が空間周期的に拡がっているため、研磨レートが初期から基板３３１のどの部分でも略等しくなり、少なくとも画素領域２０及びシール領域２２７では高精度の表面平坦性を実現できる。

【０１０５】図１６は、実施形態３において第３の層間絶縁膜１３を膜厚約２４０００Åで成膜した後、その画素領域２０の中心部の第３の層間絶縁膜１３の残膜厚が約１２０００ÅになるまでＣＭＰ処理を施した液晶パネル用基板３３１における研磨後の第３の層間絶縁膜１３の膜厚分布を示す等膜厚線図である。また、図２４中のプロット○印を連ねるグラフは図１６中のａ－ａ′線に沿うシール左辺縦方向の残膜厚の分布を示し、図２５中のプロット○印を連ねるグラフは図１６中のｂ－ｂ′線に沿う画素中央縦方向の残膜厚の分布を示し、図２６中のプロット○印を連ねるグラフは図１６中のｃ－ｃ′線に沿うシール上辺横方向の残膜厚の分布を示し、図２７中のプロット○印を連ねるグラフは図１６中のｄ－ｄ′線に沿う画素中央横方向の残膜厚の分布を示し、図２８中のプロット○印を連ねるグラフは図１６中のｅ－ｅ′線に沿う画素中央横方向の残膜厚の分布を示す。

【０１０６】これらの図から判るように、画素領域２０及びシール領域２２７（シール四隅部２２７Ｃを含む）での最大膜厚差は約８５０Åであり、基板全体での最大膜厚差は約９５０Åであった。画素領域２０及びシール領域２２７での平坦性は充分であった。なお、入力端子パッド２６の周囲領域では多少研磨不足ぎみであるため、入力端子パッド２６の周囲領域での擬似画素凹凸パターンＰのパターン密度を更に下げれば、更なる平坦化も実現できる。

【０１０７】画素での凹凸形状模様に影響する構成要素としては、フィールド酸化膜３に開けた２つの開口部、最下層配線のゲート線４、第１のメタル層のデータ線７，ソース電極配線７ａ及び中継配線１０、第２のメタル層の遮光膜１２やプラグ貫通用開口部１２ａである。本例の擬似画素凹凸パターンＰでは、最下層配線のゲート線４を第１のメタル層の擬似ゲート線４$_p$に見立てているが、画素領域２０と同様に、擬似ゲート線４$_p$を最下層配線で形成しても良い。また、擬似画素凹凸パターンＰの構成要素にフィールド酸化膜３に開けた２つの開口部に見立てた擬似開口部やプラグ貫通用開口部１２ａに見立てた擬似プラグ貫通用開口部を形成を含ませても良い。プロセス援用ができるので工数追加を招かず、画素領域２０の外側に一層リアルな擬似画素凹凸パターンを形成でき、画素領域２０及びシール領域２２７の更なる平坦化を実現できる。

【０１０８】ところで、ＣＭＰ処理においては、被研磨面の凸部が密であると初期研磨し難く、逆に被研磨面の凸部が粗であると初期研磨し易い。孤立突起は速く研磨されるからである。また、同等大きさの突起が密にランダム分布している領域と粗にランダム分布している領域とが存在する場合、粗の領域の方が初期研磨レートが速いため、研磨仕上がりでは両者領域に跨がる勾配面が形成され得る。粗の領域では結果としてパターン密度が低い。他方、被研磨面のどの部分のパターン密度が略等しくても、突起の平面規模（島状面積）が小さい領域の方が初期研磨レートが速い。島状面積に比し島状周囲（輪郭）長さが長くなるためである。従って、突起の島状面積が大きく且つ密にランダム分布している領域が一番初期研磨し難い。その極限例が領域全体に連続拡張面（いわゆるベタ）が形成されている場合である。逆に、突起の島状面積が小さく且つ粗にランダム分布している領域は一番初期研磨し易い。その極限例が領域全体に突起がない（ダミーパターンがない）場合である。しかし、突起の島状面積が大きく且つ粗にランダム分布している領域や突起の島状面積が小さく且つ密に分布している領域は、上記の最高研磨レートと最低研磨レートとの中間の初期研磨レートであろうが、突起の島状面積が大きく且つ粗にランダム分布している領域と、突起の島状面積が小さく且つ密にランダム分布している領域とは、いずれの方が速い初期研磨レートであるか否かは、研磨液や他の条件（分布の規則性，突起形状，突起配列，突起配置など）にも起因しているため、判然としない。ただ、実際のＣＭＰ処理では砥液が画素領域２０の凹凸の規則的分布によりある程度規則的な流動分布を引き起こしているものと考えられるため、非画素領域でも同様な流動分布となるように工夫する必要もある。

【０１０９】実際、反射型液晶パネル用基板のチップサイズ内においては、入力端子パッド２６が最も広い島状突起でその１次元配列の間隔からして粗の分布と考えられるので、この入力端子パッド２６を含む領域が最高研磨レートとなる。ところが、画素領域２０では画素凹凸パターンが縦横２次元にマトリクス状に展開された明瞭な空間周期性を呈している。従って、画素領域２０の凹凸分布には、画素凹凸パターンの空間周期性という高次の規則性と画素凹凸パターン内の低次の規則性とから成

る階層的規則が存在する。画素凹凸パターンは、１０００Å～１００００Å程度の微細な線幅に代表される微視的な各種の基本（１次）凹凸部（フィールド酸化膜３に開けた２つの開口部，最下層配線のゲート線４，第１のメタル層のデータ線７，ソース電極配線７ａ，及び中継配線１０，第２のメタル層の遮光膜１２やプラグ貫通用開口部１２ａ）の分布と、画素中でこれら基本凹凸部の偏りにより生じる凹凸密集部（２次凹凸部）とから成る階層構造と考えられる。本例の擬似画素凹凸パターンＰでは、この基本凹凸部に逐一忠実に対応させた原始的な基本凹凸部をそのまま模する代わりに、マクロ的な凹凸密集部を見立てるように、擬似ゲート線4_p，擬似データ線7_p，擬似ソース電極配線$7a_p$及び擬似中継配線10_pのみを形成したものである。本例の凹凸密集部としては、ゲート線４とデータ７との重なり部分や容量電極９ａと中継配線１０の重なり部分が考えられる。このため、擬似画素凹凸パターンＰは擬似ゲート線4_p，擬似データ線7_p及び擬似中継配線10_pを含むことが好ましい。典型的な凹凸部分を擬似画素凹凸パターンＰの要素とすれば良い。擬似画素凹凸パターンＰの中での典型的な凹凸部分の位置と実際の画素の中の典型的な凹凸部分位置とが正確に対応していなくても構わない。

【０１１０】ここで例えば、画素凹凸パターンが３次以上の階層構造と考えられる場合、基本凹凸部の細密なデットコピーまでは必要でなく、巨視的な階層から３次又は２次凹凸部までを模するだけでも充分であろう。ただ、このような画素内の凹凸パターンの階層構造が明瞭でない場合、基本凹凸部のデッドコピーを擬似画素凹凸パターンＰとする方がマスク設計上の煩雑さを回避できる利点がある。また、最大膜厚差が１０００Å以下となるような更なる高精度の平坦化を企画する場合は、画素のデッドコピーを擬似画素凹凸パターンＰとする方が良い。

【０１１１】なお、上記の実施形態の液晶パネル基板は反射型液晶パネルに用いるに好適であるが、その反射型液晶パネルは前述した液晶プロジェクタのライトバルブは勿論のこと、腕時計型電子機器、ワードプロセッサ，パーソナルコピュータ等の携帯型情報処理機、携帯電話機の表示部やその他各種の電子機器の表示部に適用することができる。

【０１１２】また、上記実施形態の液晶パネル基板は半導体基板の主面にスイッチング素子を作り込んだものであるが、半導体基板に限らず、基板としてはガラス基板や石英基板等の絶縁性基板を用いることができる。スイッチング素子として絶縁性基板上に薄膜トランジスタ（ＴＦＴ）などを形成する場合でも、本発明を適用できることは言う迄もない。

【０１１３】更に、本発明は液晶パネル基板に限らず、他のフラットディスプレイ用基板に適用できるものである。

【０１１４】

【発明の効果】以上説明したように、本発明は、画素領域の空き間にダミーパターンを割り込ませて形成するのではなく、逆に、非画素領域において既成導電層層を援用して被研磨層の上層の層間絶縁膜の底上げ用のダミーパターンを略一面的に形成した点を特徴とするものである。画素領域においてダミーパターンを形成する場合は、底上げのための中間導電層と層間絶縁膜との成膜工程を追加せねばならず、また、研磨前の層間絶縁膜の表面起伏が抑えられていると、却って初期研磨レートが低くなるので、層間絶縁膜表面を鏡面様に平坦化するために必要な研磨時間が長くなり、砥液の消費も増大する。しかしながら、本発明は上記の不都合を解消できるばかりか、次のような効果を奏する。

【０１１５】（１）　端子パッドの近傍に、単層又は複層のダミーパターンを有する場合、端子パッドの近傍の上層の層間絶縁膜の成膜表面レベルが画素領域での成膜表面レベルと略同等レベルになり、表面レベルが全体として均一化するため、研磨処理において一様の研磨レートが得られる。このため、従前の成膜表面レベルが均一化されていない状態で問題となっていた端子パッド部の易研磨性が改善され、端子パッド部の下地が露出することがない。これは画素領域表面の更なる鏡面様の平坦化に役立ち、且つ研磨処理前の層間絶縁膜の薄膜化も実現できる。この薄膜化により、画素領域にある層間導電部のコンタクトホールのアスペクト比を改善できるので、コンタクトホールの細径化により開口部の細径化に結び付けることができる。それ故、遮光性能が向上し、スイッチング素子特性を改善できる。勿論、成膜工数の追加を招かずに済む。

【０１１６】そして、画素領域外の端子パッドの近傍域にも導電層のダミーパターンが敷き詰められていると、このダミーパターンも遮光膜となるため、迷光が画素領域外から基板に作り込んだ素子領域に入り難くなり、光電流を抑制でき、スイッチング素子の改善に役立つ。

【０１１７】（２）　入力端子パッドの周囲に配置されたダミーパターンが平面的に細分化された複数の小分けダミーパターンからなる場合、成膜直後の層間絶縁膜の表面レベルを均一化しながら、隣接の端子パッド間のショートを防止できる。

【０１１８】（３）　相隣り合う入力端子パッド間が非ダミーパターン領域である場合、入力端子パッド間のショートを確実に防止できる。

【０１１９】（４）　この入力端子パッドとその周囲に配置された小分けダミーパターンとの間隔が、配線とその近傍のダミーパターンとの間隔よりも広く設定されてなる場合、異方性導電膜の導電性粒子による入力端子パッドと小分けダミーパターンとの架橋が起こり難くなり、ショートを極力防止できる。

【０１２０】（５）　中継端子パッドとその周囲に配置

されたダミーパターンとの間隔が、配線とその近傍のダミーパターンとの間隔よりも広く設定されている場合、中継端子パッド上では通常銀ペーストで導通が図られるようになっているが、銀ペーストが中継端子パッドから若干はみ出しても、その近傍のダミーパターンにショートし難くなる。

【０１２１】（６） 端子パッドの近傍域に限らず、画素領域の周囲を取り囲むシール領域に、ダミーパターンが形成されている場合、その部分の研磨処理前の層間絶縁膜の表面は画素領域のそれと略同等になるので、研磨処理によって平坦化を行う際、画素領域はその周辺部まで均一なレートで研磨が進行する。このため、従前に比べ画素領域の平坦性が一層良好となり、反射率が向上するだけでなく、研磨後のコンタクトホールのエッチング時間が決定し易くなる。

【０１２２】（７） 更に、ダミーパターンをシール領域の外周部にも設けることにより、この領域はシール領域部分の上層の層間絶縁膜の表面のレベルと同等になる。従って研磨した場合、シール領域の層間絶縁膜表面が勾配面となることはなく、シール材の密着性を改善することができる。

【０１２３】（８） シール領域のダミーパターンがスイッチング素子の制御配線層と同層で孤立したパターンの上に積み足されて成る場合、研磨処理の層間絶縁膜の表面レベルの平坦化を更に微細に調節できる。

【０１２４】（９） そして、画素領域の周辺に配置され、スイッチング素子に信号を供給する駆動回路の近傍領域に、ダミーパターンを積み重ねて成る場合、研磨処理の層間絶縁膜の平坦化等に役立つ。

【０１２５】（10） 更に、本発明においては、画素領域を取り囲むシール領域の隅部領域には、シール領域の辺領域又は当該隅部の周辺領域よりも密度の低い分布でダミーパターンが形成されている。このため、シール四隅部における研磨前の層間絶縁膜の表面は離散的な複数のダミーパターンによる凹凸が反映した面粗さを呈しており、研磨処理を施すと、シール領域の辺部の平坦に近い起伏に比し四隅部の初期研磨レートが速くなるため、これに引きずられる形で四隅部で囲まれたシール領域内側の研磨レートが略平等化する傾向で進行し、画素領域及びシール領域の残膜厚バラツキが抑制される。

【０１２６】（11） また、シール四隅部において全くダミーパターンがない（パターン密度ゼロ）場合でも、隅部領域が落ち込みその境界部分が立ち上がっているため、研磨初期ではその境界部分が勾配面となり、その勾配面が次第に内方へ波及する。

【０１２７】従って、画素領域及びシール領域の全体的な平坦化を得ることができる。

【０１２８】（12） そしてまた、本発明においては、非画素領域に連続拡張面（いわゆるベタ）のダミーパターンを形成するではなく、画素の凹凸を模した複数の擬似画素凹凸パターンを形成した構成を採用できる。研磨処理前の層間絶縁膜の画素領域以外の表面にも、画素の表面凹凸模様と殆ど類似の表面凹凸模様が拡がっているため、研磨レートが初期から基板のどの部分でも略等しくなり、少なくとも画素領域及びシール領域では高精度の表面平坦性を実現できる。

【０１２９】（13） 複数の擬似画素凹凸パターンを非画素領域上に２次元方向に繰り返し展開形成した構成では、画素領域のマトリクス状などの空間規則性も対応することになるため、画素領域及びシール領域での表面平坦性が顕著になる。

【０１３０】（14） この擬似画素凹凸パターンが少なくとも擬似ゲート線，及び擬似データ線で構成されて成る場合、画素の凹凸の顕著な（代表的）部分や画素領域の凹凸規則性に最も酷似するパターンとなるので、画素領域及びシール領域での層間絶縁膜を高精度に平坦化できる。

【図面の簡単な説明】

【図１】本発明の実施形態１に係る反射型液晶パネルの反射型液晶パネル用基板のレイアウト構成例を示す平面図である。

【図２】図１中のＢ－Ｂ′線に沿って切断した状態を示す切断図である。

【図３】図２の断面構造に対し端子パッドの構造を変えた状態を示す断面図である。

【図４】実施形態１の反射型液晶パネル用基板において画素領域とシール領域の近辺を示す部分平面図である。

【図５】実施形態１の反射型液晶パネル用基板においてデータ線駆動回路の近辺を示す部分平面図である。

【図６】実施形態１の反射型液晶パネル用基板において端子パッドの近辺を示す部分平面図である。

【図７】実施形態１の反射型液晶パネル用基板における端子パッドとフレキシブルテープ電線との接続状態を示す部分平面図である。

【図８】図７中のＡ－Ａ′線に沿って切断した状態を示す切断図である。

【図９】実施形態１の反射型液晶パネル用基板において中継端子パッドの近辺を示す部分平面図である。

【図１０】実施形態１において第３の層間絶縁膜を膜厚約２４０００Åで成膜した後、その画素領域の中心部の第３の層間絶縁膜の残膜厚が約１２０００ÅになるまでＣＭＰ処理を施した液晶パネル用基板における研磨後の第３の層間絶縁膜の膜厚分布を示す等膜厚線図である。

【図１１】本発明の実施形態２に係る反射型液晶パネル用基板においてシール領域の四隅部の近辺を示す部分平面図である。

【図１２】図１１中のＣ－Ｃ′線に沿って切断した状態を示す断面図である。

【図１３】実施形態２において第３の層間絶縁膜を膜厚約２４０００Åで成膜した後、その画素領域の中心部の

第３の層間絶縁膜の残膜厚が約１２０００ÅになるまでＣＭＰ処理を施した液晶パネル用基板における研磨後の第３の層間絶縁膜の膜厚分布を示す等膜厚線図である。

【図１４】本発明の実施形態３に係る反射型液晶パネル用基板においてシール領域の四隅部の近辺を示す部分平面図である。

【図１５】図１４中のＣ－Ｃ′線に沿って切断した状態を示す断面図である。

【図１６】実施形態３において第３の層間絶縁膜を膜厚約２４０００Åで成膜した後、その画素領域の中心部の第３の層間絶縁膜の残膜厚が約１２０００ÅになるまでＣＭＰ処理を施した液晶パネル用基板における研磨後の第３の層間絶縁膜の膜厚分布を示す等膜厚線図である。

【図１７】反射型液晶パネルをライトバルブとして用いた投写型表示装置の一例としてビデオプロジェクタを示す概略構成図である。

【図１８】反射型液晶パネルを示す断面図である。

【図１９】従来の反射型液晶パネルに用いる反射型液晶パネル用基板を示す平面図である。

【図２０】図１９の反射型液晶パネル用基板の画素領域を示す部分平面図である。

【図２１】図１３中のＡ－Ａ′線に沿って切断した状態を示す切断図である。

【図２２】図１２中のＢ－Ｂ′線に沿って切断した状態を示す切断図である。

【図２３】図１９に示す従来の反射型液晶において第３の層間絶縁膜を膜厚約２４０００Åで成膜した後、その画素領域の中心部の第３の層間絶縁膜の残膜厚が約１２０００ÅになるまでＣＭＰ処理を施した液晶パネル用基板における研磨後の第３の層間絶縁膜１３の膜厚分布を示す等膜厚線図である。

【図２４】図２３の従来例，図１０の実施形態１，図１３の実施形態２及び図１６の実施形態３において、ａ－ａ′線に沿うシール左辺縦方向の残膜厚の分布をそれぞれ示すグラフである。

【図２５】図２３の従来例，図１０の実施形態１，図１３の実施形態２及び図１６の実施形態３において、ｂ－ｂ′線に沿う画素中央縦方向の残膜厚の分布をそれぞれ示すグラフである。

【図２６】図２３の従来例，図１０の実施形態１，図１３の実施形態２及び図１６の実施形態３において、ｃ－ｃ′線に沿うシール上辺横方向の残膜厚の分布をそれぞれ示すグラフである。

【図２７】図２３の従来例，図１０の実施形態１，図１３の実施形態２及び図１６の実施形態３において、ｄ－ｄ′線に沿う画素中央横方向の残膜厚の分布をそれぞれ示すグラフである。

【図２８】図２３の従来例，図１０の実施形態１，図１３の実施形態２及び図１６の実施形態３において、ｅ－ｅ′線に沿う画素中央横方向の残膜厚の分布をそれぞれ示すグラフである。

【符号の説明】

１…Ｐ⁻⁻型半導体基板
２，２１′…Ｐ型ウェル領域
３…フィールド酸化膜
４…ゲート線
４ａ…ゲート電極
４ｂ…ゲート絶縁膜
4_p …擬似ゲート線
５ｂ…N^+ 型ドレイン領域
６…第１の層間絶縁膜
６ａ，６ｂ，６ｃ，１６…コンタクトホール
７…データ線
７ａ…ソース電極配線
7_p …擬似データ線
$7a_p$ …擬似ソース電極配線
８…Ｐ型容量電極領域
９ａ…容量電極
９ｂ…絶縁膜（誘電膜）
１０…中継配線
１１…第２の層間絶縁膜
１２…遮光膜
１２ａ…プラグ貫通用開口部
１２ｂ…接続用配線
12_p …擬似遮光膜
１３…第３の層間絶縁膜
１４…画素電極
１５…接続プラグ（層間導電部）
１７…パッシベーション膜
２０…画素領域（表示領域）
２１…データ線駆動回路（Ｘドライバ）
２２Ｒ，２２Ｌ…ゲート線駆動回路（Ｙドライバ）
２３…プリチャージ及びテスト回路
２４…画像信号サンプリング回路
２５…遮光膜
２６，２６′…入力端子パッド
２６ａ…下層
２６ｂ，２６ｂ′…上層
２７，１２７，２２７…シール領域
２９Ｒ，２９Ｌ…中継端子パッド（銀点）
３０…反射型液晶パネル
３１，１３１，２３１，３３１…反射型液晶パネル用基板
３２…支持基板
３３…対向電極（共通電極）
３５…ガラス基板
３７…液晶
３８…異方性導電膜（ＡＣＦ）
３８ａ…導電性粒子
３８ｂ…接着用絶縁樹脂材

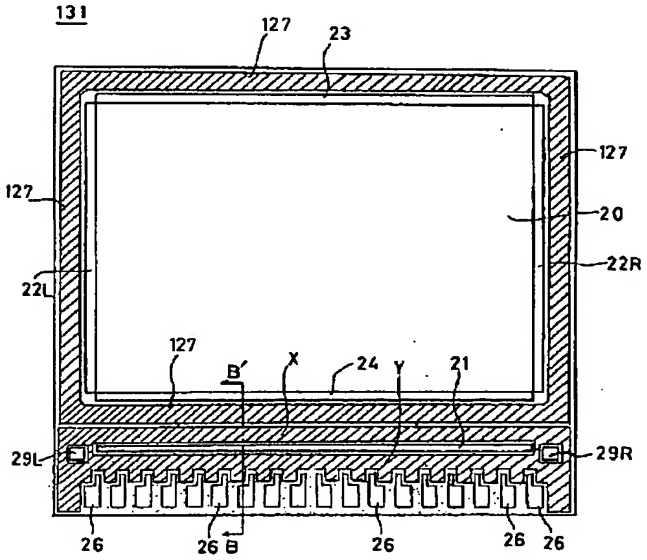
35

３９…フレキシブルテープ配線
３９ａ…フレキシブルテープ
３９ｂ…導電線
１００…偏光照明装置
１１０…インテグレートレンズ
１２７ａ…パターン
１２７Ｃ，２２７Ｃ…四隅部
１３０…偏光変換素子
２００…偏光ビームスプリッタ
２０１…Ｓ偏光束反射面
２６１…導電接触部
２６２…配線引出し部
４１２，４１３…ダイクロイックミラー
３００Ｂ，３００Ｒ，３００Ｇ…反射型液晶ライトバルブ

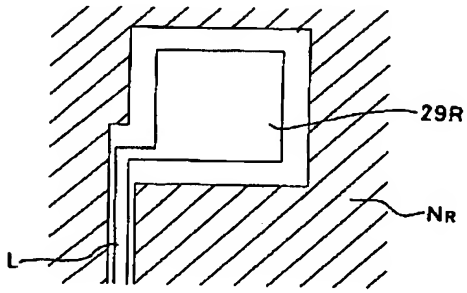
36

５００…投写光学系
６００…スクリーン
L_0 …システム光軸
Ａ…下層ダミーパターン
Ｂ，Ｂ′…上層ダミーパターン
ａ…小分けダミーパターン
Ｘ，Ｘ′，Ｙ…挟間領域
Ｗ…行方向配線領域
Ｌ，L_{IN}，L_{OUT} …配線
Ｍ，Ｔ…配線間ダミーパターン
N_R，N_L …ダミーパターン
S_0，S_1，S_2，S_2′，S_3 …小分けダミーパターン
Ｐ…擬似画素凹凸パターン

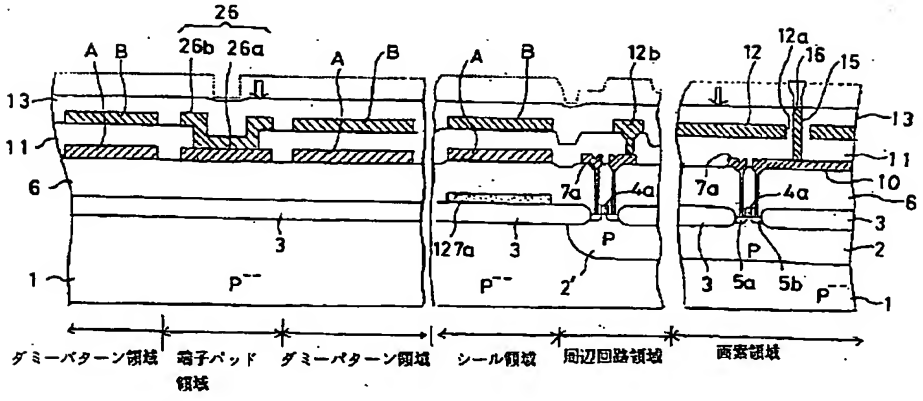
【図１】



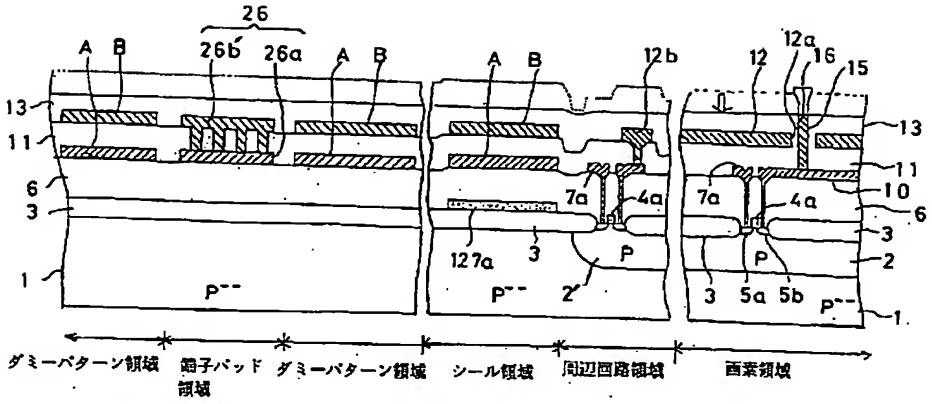
【図９】



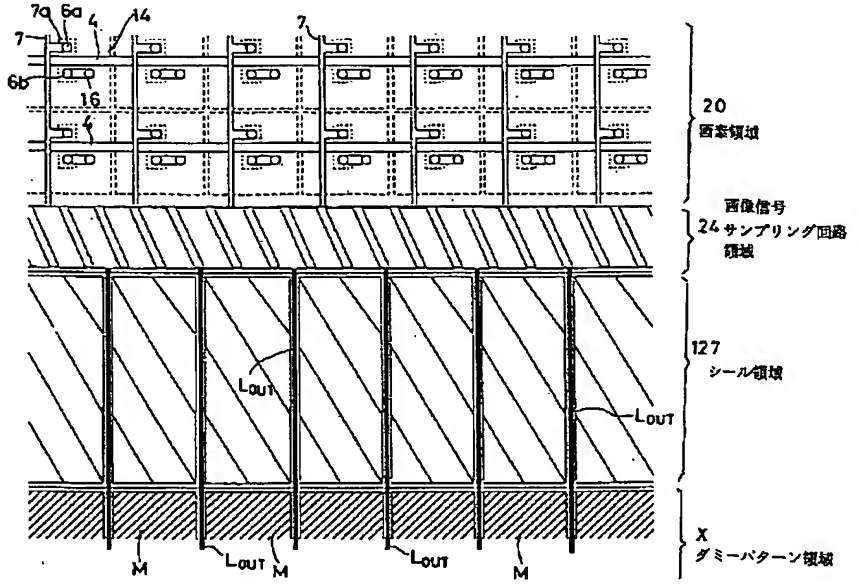
【図２】



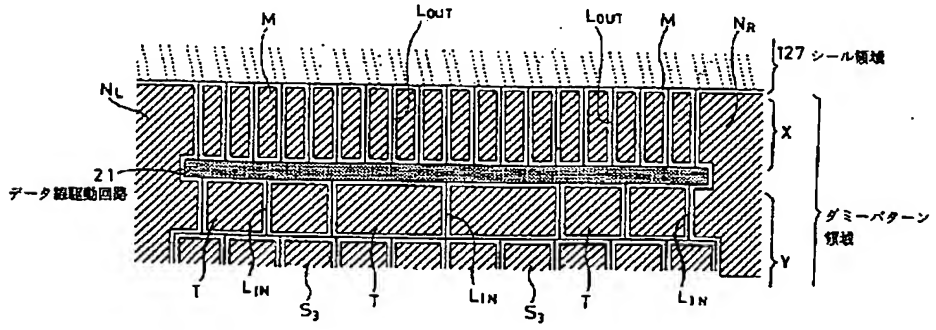
【図３】


26
A B
26b 26a
12b
12a
16
15
12
13
11
6
3
1
7a
4a
127a
P
P--
2
5a 5b
10
2
ダミーパターン領域
端子パッド領域
ダミーパターン領域
シール領域
周辺回路領域
画素領域

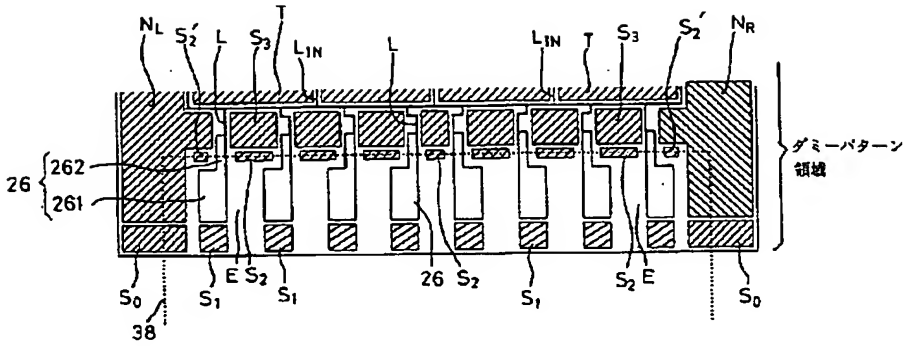
【図４】


7a 6a
4
14
7
6b
16
20
画素領域
画像信号
24 サンプリング回路領域
127
シール領域
LOUT
M
X
ダミーパターン領域

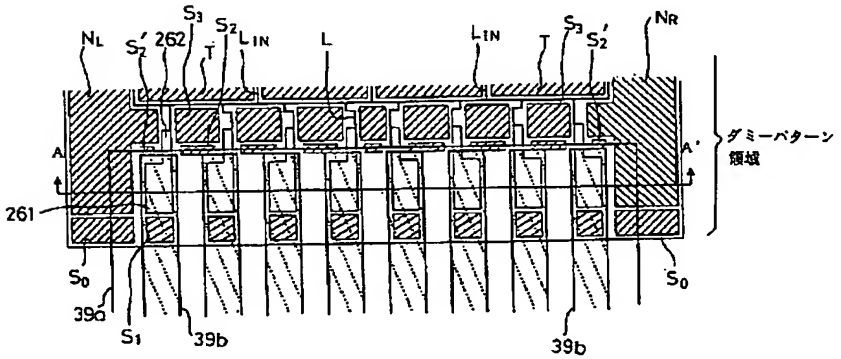
【図５】


M
LOUT
NR
NL
127 シール領域
X
21
データ線駆動回路
ダミーパターン領域
Y
T
LIN
S3

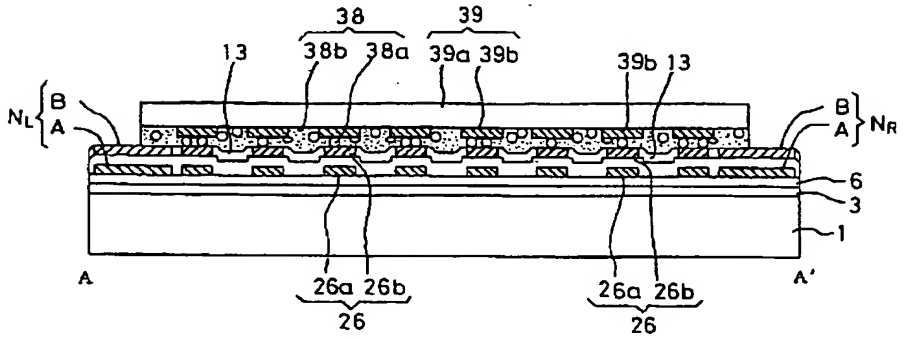
【図６】


N_L
S_2'
L
S_3
T
L_IN
L
L_IN
T
S_3
S_2'
N_R
ダミーパターン領域
26
262
261
S_0
38
S_1
E
S_2
S_1
26
S_2
S_1
S_2
E
S_0

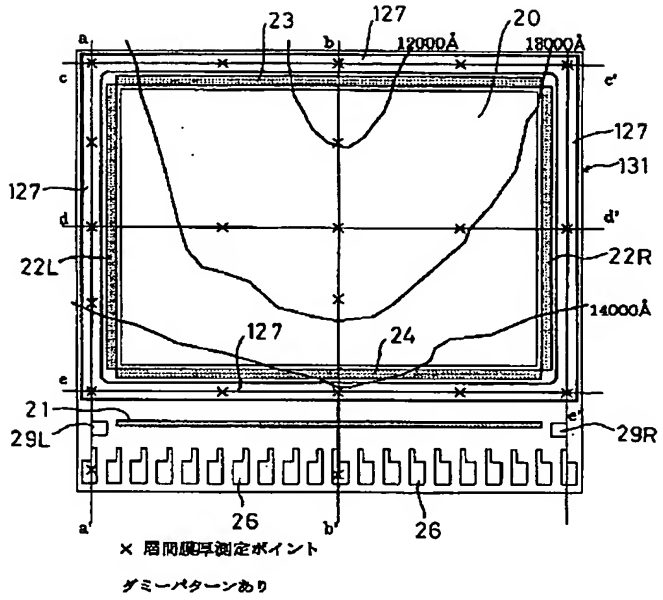
【図７】


N_L
S_2'
262
S_3
S_2
T
L_IN
L
L_IN
T
S_3
S_2'
N_R
ダミーパターン領域
A
A'
261
S_0
39a
S_1
39b
39b
S_0

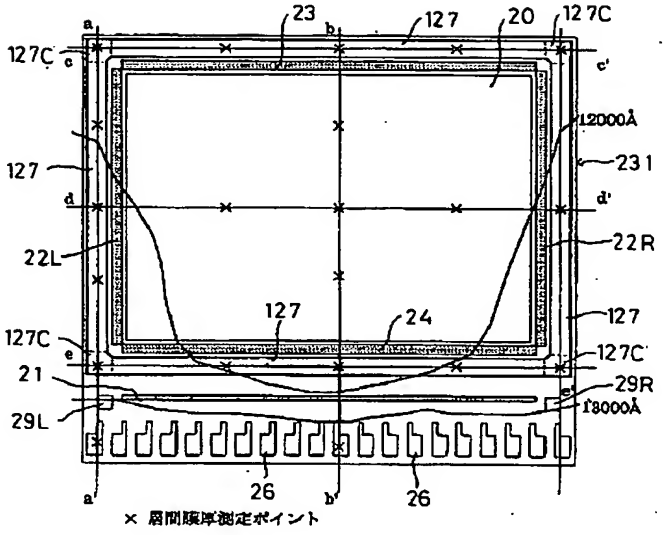
【図８】


38
39
13
38b
38a
39a
39b
39b
13
N_L
B
A
B
A
N_R
6
3
1
A
A'
26a
26b
26
26a
26b
26

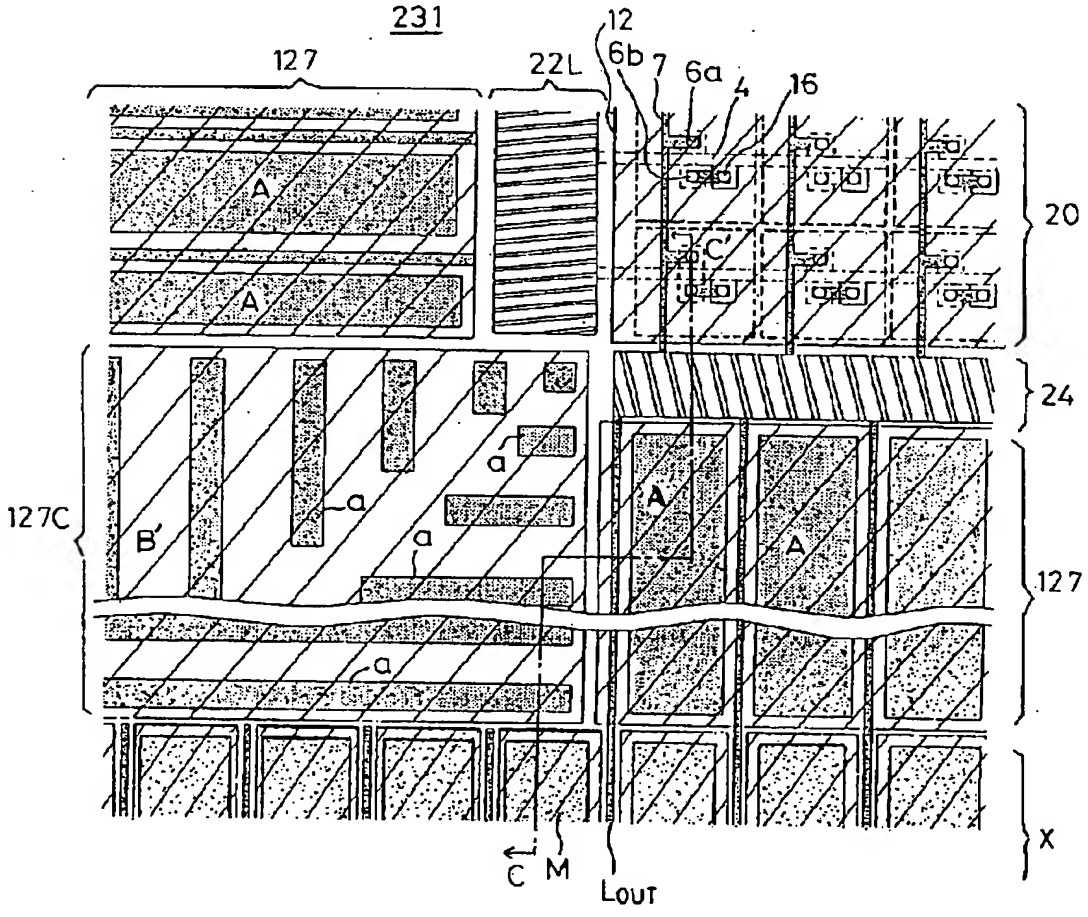
【図１０】


23
127
20
12000Å
18000Å
127
131
22L
22R
14000Å
24
21
29L
29R
26
26
× 層間膜厚測定ポイント
ダミーパターンあり

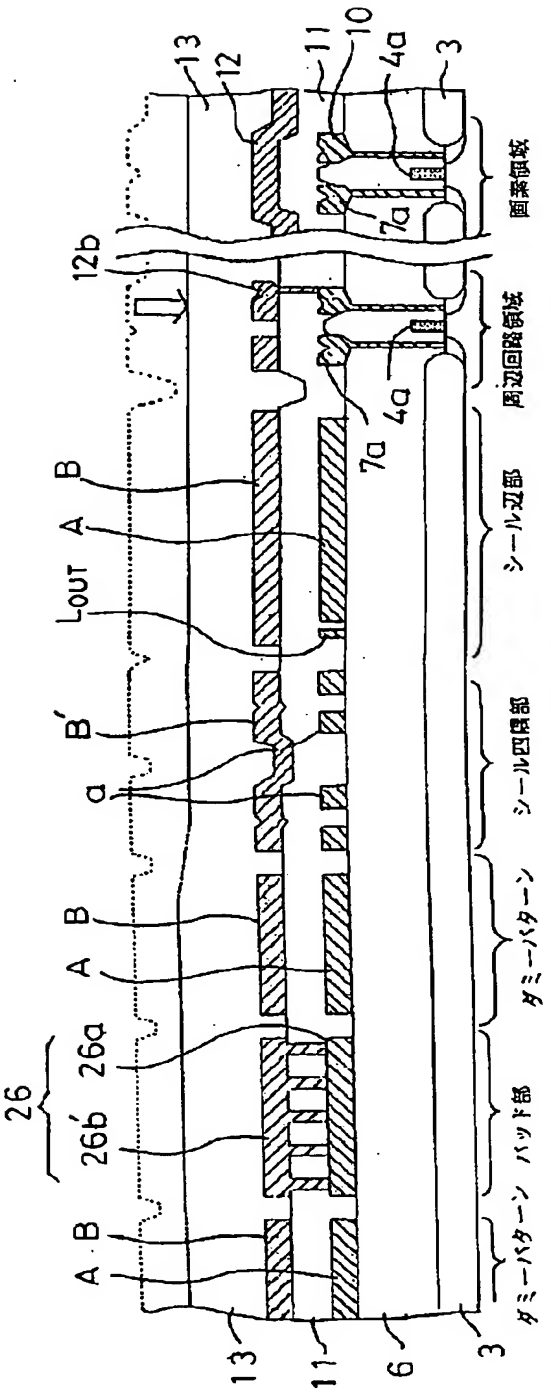
【図１３】


23
127
20
127C
12000Å
231
22L
22R
24
21
29L
29R
18000Å
26
26
× 層間膜厚測定ポイント

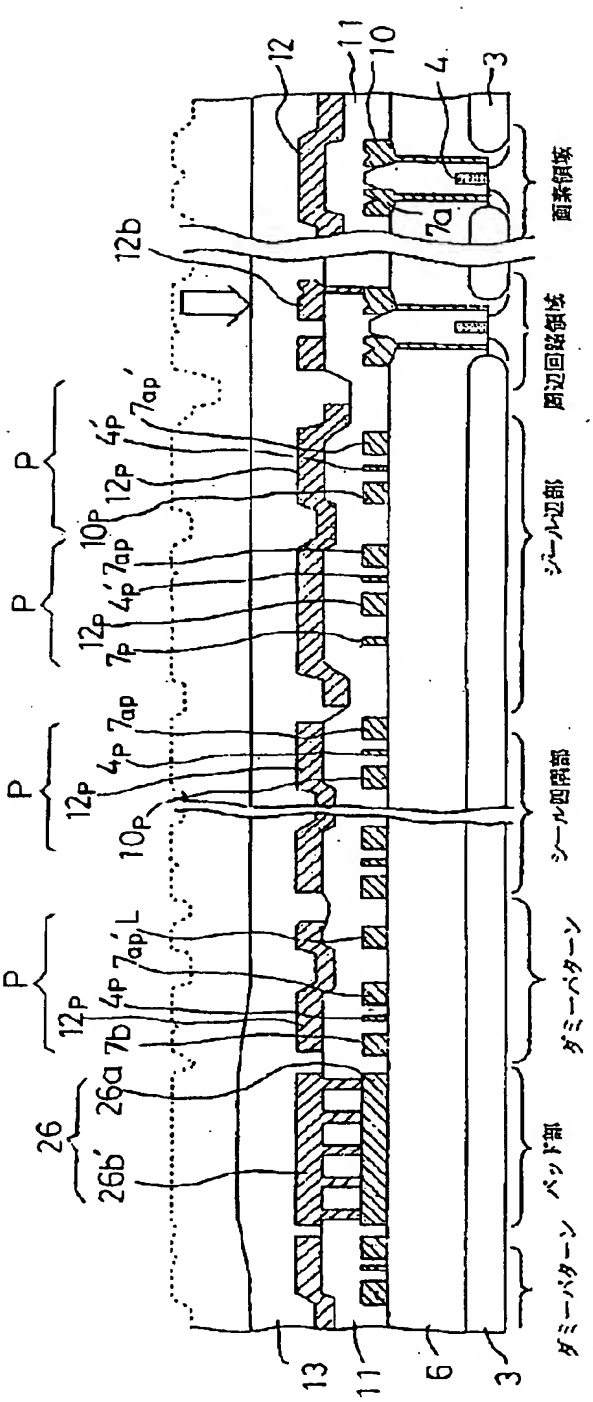
【図１１】


231
127
22L
12
6b
7
6a
4
16
20
24
127C
127
X
A
A'
B'
a
C
M
LOUT

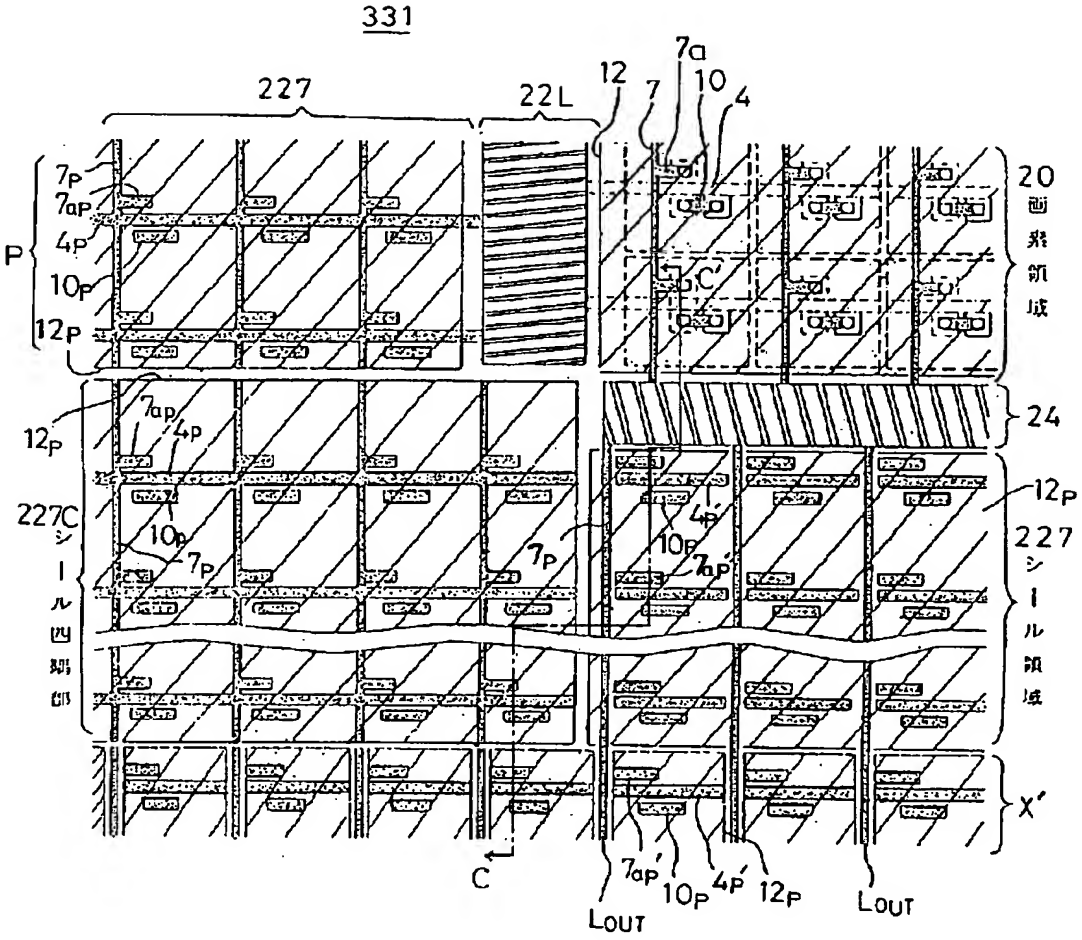
【図１２】


26
26b
26a
A
B
A
B
a
B'
Lout
A
B
12b
13
12
11
10
4a
3
7a
4a
7a
A
B
画素領域
周辺回路領域
シール辺部
シール四隅部
ダミーパターン
パッド部
ダミーパターン
13
11
6
3

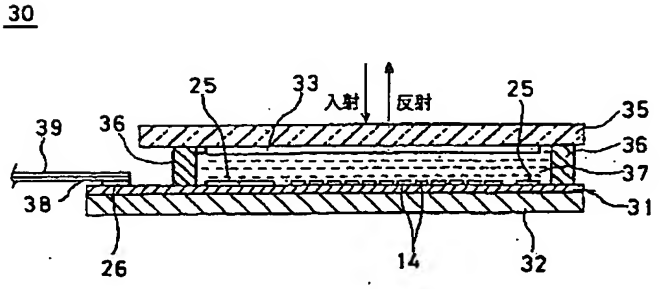
【図１５】


26
26b'
26a
7b
12P
4P
7ap'L
P
12P
4P
7ap
P
12P
7P
4'P
12P
10P
7ap
4'P
7ap'
P
10P
12b
12
11
10
4
3
7a
画素領域
周辺回路領域
シール辺部
シール四隅部
ダミーパターン
パッド部
ダミーパターン
13
11
6
3

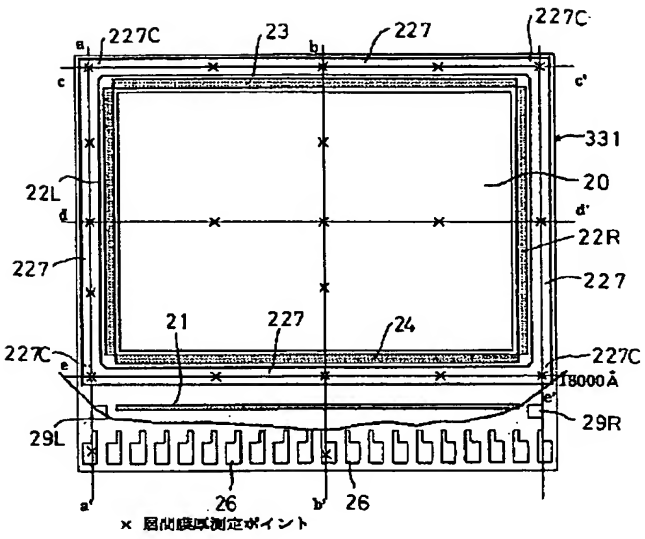
【図１４】


331
227
22L
12
7
7a
10
4
20
画素領域
24
227
シール領域
227C
シール四辺部
X'
C
C'
P
7P
7aP
4P
10P
12P
LOUT

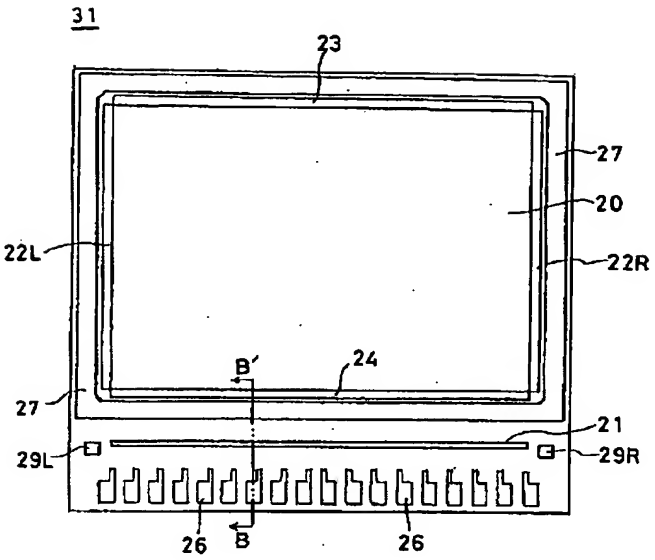
【図１８】


30
25
33
入射
反射
25
35
39
36
36
37
38
31
26
14
32

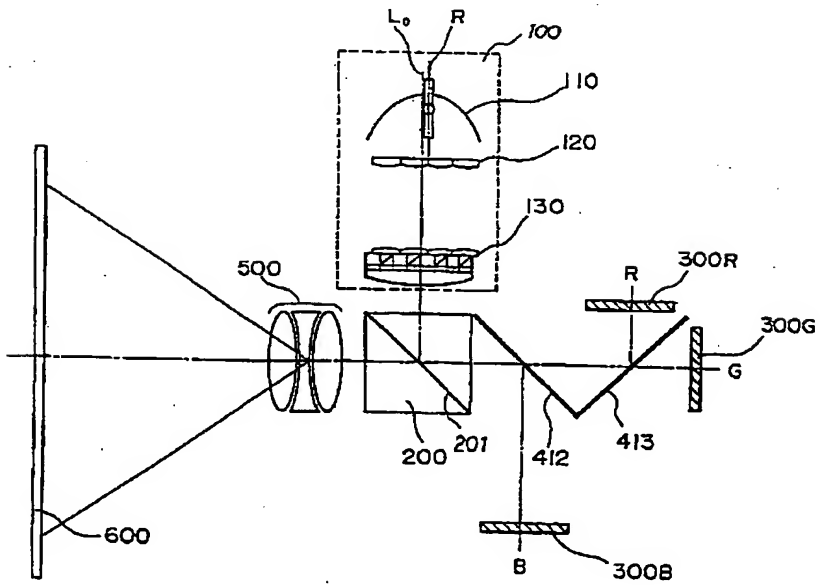
【図１６】


227C
23
227
227C
331
20
22L
22R
227
21
227
24
227C
18000Å
29L
29R
26
26
× 層間膜厚測定ポイント

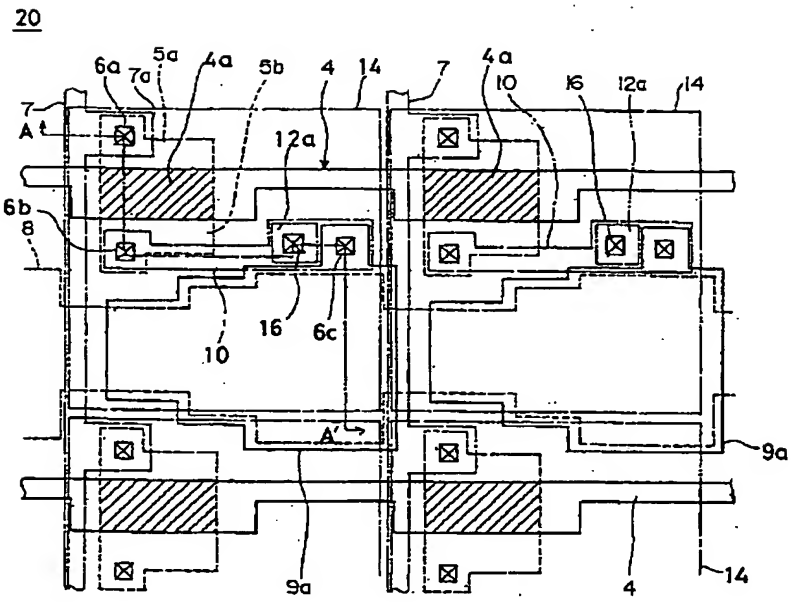
【図１９】


31
23
27
20
22L
22R
B'
24
27
21
29L
29R
26
B
26

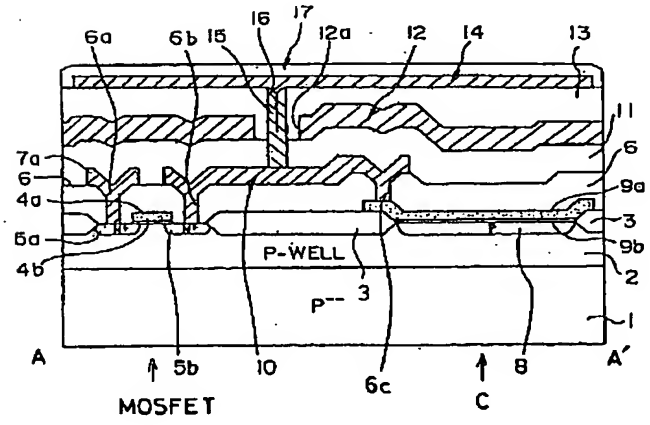
【図１７】


L₀
R
100
110
120
130
500
R
300R
300G
G
200
201
412
413
600
B
300B

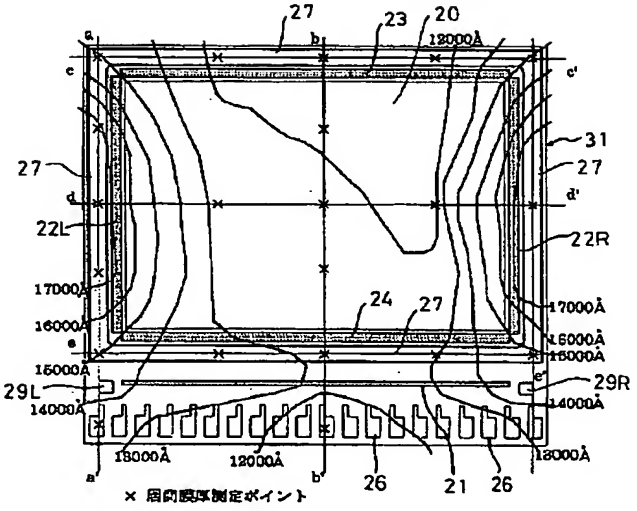
【図２０】


20
6a
7a
5a
4a
5b
4
14
7
4a
10
16
12a
14
7
A
12a
6b
8
16
6c
10
A'
9a
9a
4
14

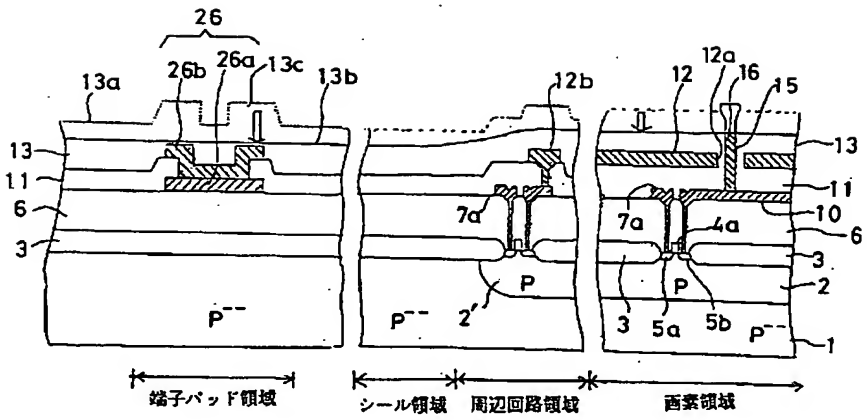
【図２１】


6a
6b
15
16
17
12a
12
14
13
11
6
9a
3
9b
2
1
7a
6
4a
5a
4b
P-WELL
P-- 3
A
5b
10
6c
8
A'
MOSFET
C

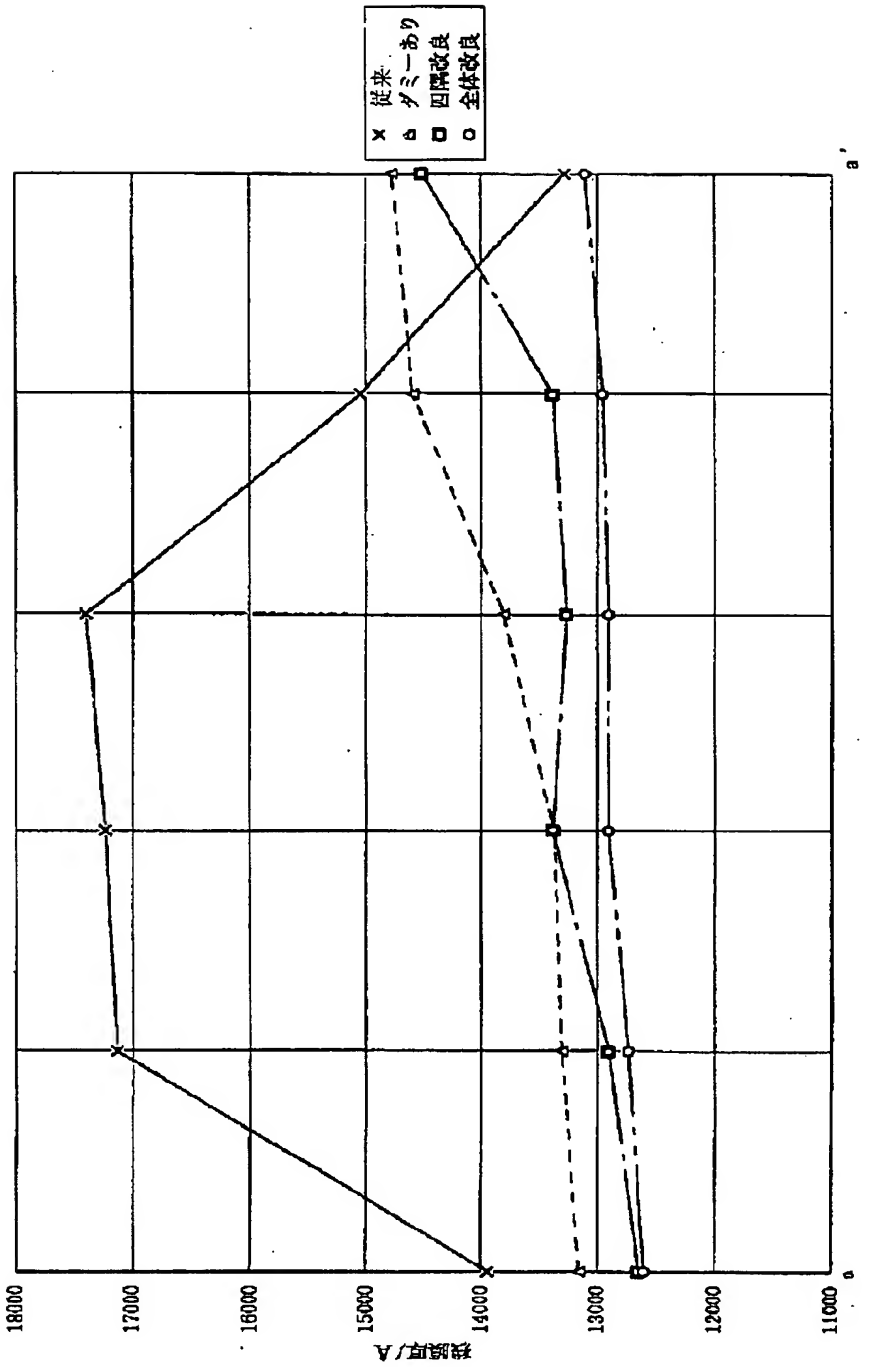
【図２３】


27
23
20
12000Å
a
b
c
c'
31
27
d
d'
22L
22R
17000Å
16000Å
24
27
e
e'
15000Å
29L
29R
14000Å
13000Å
12000Å
a'
b'
26
21
26
× 回折膜厚測定ポイント

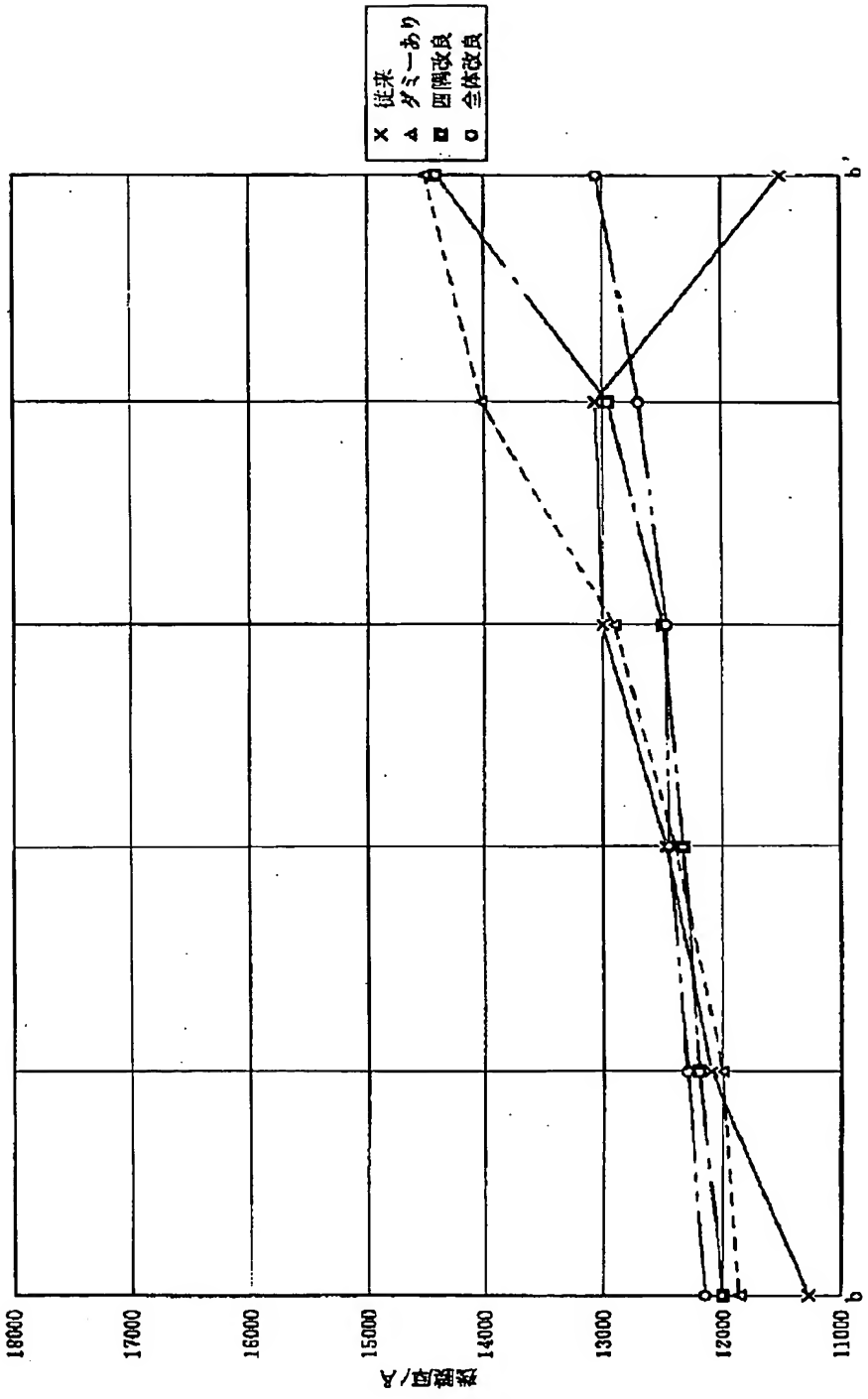
【図２２】


26
26b
26a
13c
13a
13b
12b
12
12a
16
15
13
11
6
3
7a
4a
10
P
P--
2
5a
5b
1
端子パッド領域
シール領域
周辺回路領域
画素領域

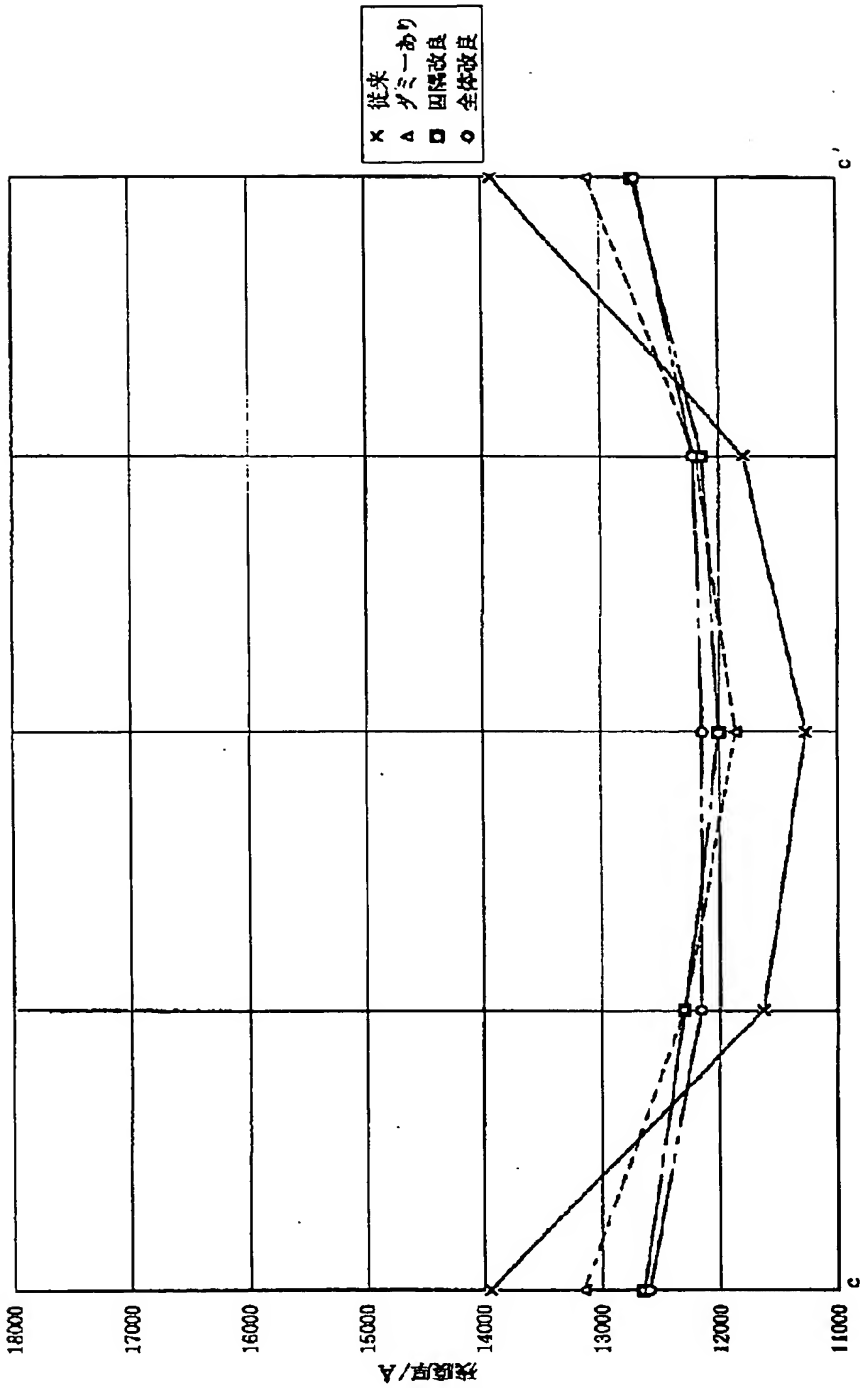
【図２４】


従来
ダミーあり
四隅改良
全体改良
a
a'
18000
17000
16000
15000
14000
13000
12000
11000
残留応力A

【図２５】


× 従来
▲ ダミーあり
■ 四隅改良
○ 全体改良
b'
b
18000
17000
16000
15000
14000
13000
12000
11000
降伏荷重/A

【図２６】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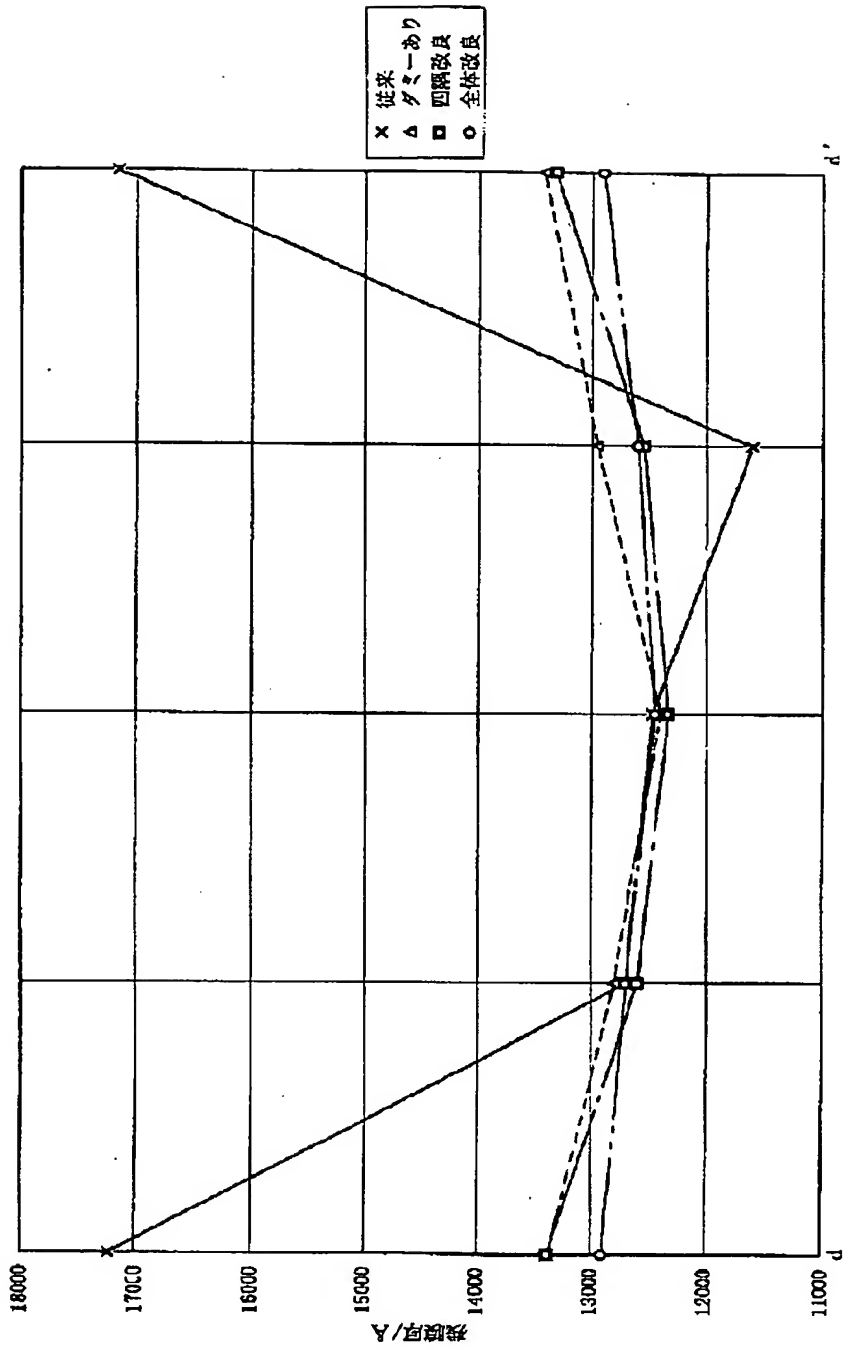
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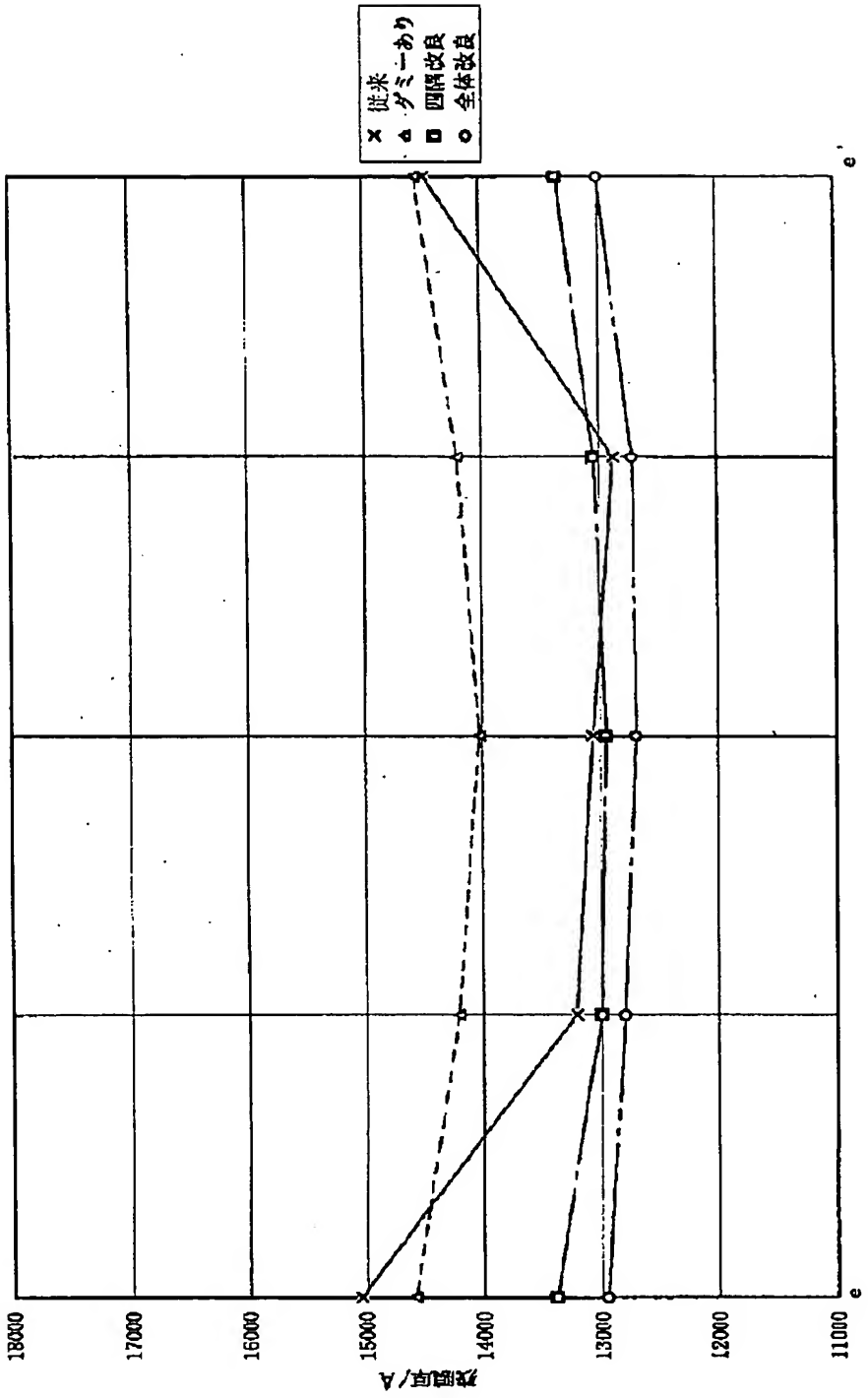
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PATENT ABSTRACTS OF JAPAN

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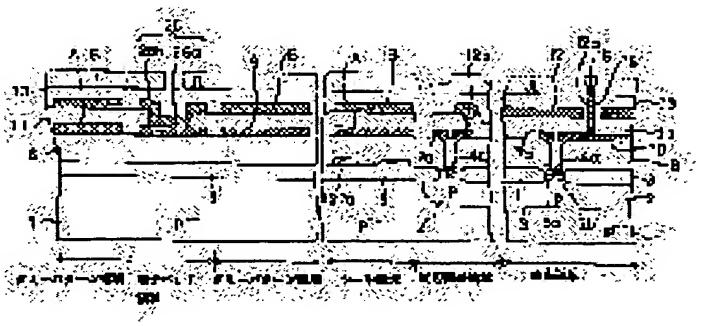
(54) SUBSTRATE FOR ELECTRO-OPTIC DEVICE, ELECTRO-OPTIC DEVICE, ELECTRONIC APPARATUS AND PROJECTION TYPE DISPLAY DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To embody a structure capable of achieving the uniformization of a polishing rate without increasing the film thicknesses of interlayer insulating films relating to the films to be polished with a substrate for a liquid crystal panel having a laminated film structure obtd. by alternately and repetitively depositing the interlayer insulating films and metallic layers on a semiconductor substrate into which element regions of transistors for pixel selection are built.

SOLUTION: This substrate for the liquid crystal panel has connecting plugs 15 for conducting and connecting wiring films 10 consisting of the first metallic layer across the second interlayer insulating film 11 under a lightproof film through apertures 12a opened at the lightproof film 12 consisting of the second material layer in the pixel regions and pixel electrodes consisting of the third metallic layer across the third interlayer insulating film 13 on the lightproof film. Lower layer dummy patterns A consisting of the first metallic layer and the upper layer dummy patterns B consisting of the second metallic layer are superposed and formed on the circumferences of the input terminal pads 26 of the non-pixel regions. Since the level of the deposition surface of the third interlayer insulating film 13 on the dummy patterns A, B is raised, the excessive polishing in these parts may be eliminated. The uniform polishing rate is, therefore, obtd. in CMP treatment.



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CLAIMS

[Claim(s)]
[Claim 1] In the pixel field to which the switching element corresponding to each pixel is arranged on a substrate It has the laminating membrane structure to which the laminating of two or more interlayer insulation films and two or more conductive layers was carried out by turns. It is the substrate for electro-optic devices with which flattening of said much more lower layer interlayer insulation film is carried out, and it consists of the conductive layer of the maximum upper layer of these two or more conductive layers by polish processing at least. The substrate for electro-optic devices characterized by having the dummy pattern of the monolayer which consists of said lower layer conductive layer formed in the non-pixel field on said substrate, or a double layer, and consisting of the interlayer insulation film of said polish processing at least near the terminal pad.
[Claim 2] Said dummy pattern which said terminal pad is an input terminal pad arranged near the substrate edge in claim 1, and has been arranged around said input terminal pad is a substrate for electro-optic devices characterized by consisting of two or more subdivision dummy patterns subdivided superficially.
[Claim 3] It is the substrate for electro-optic devices characterized by being a non-dummy pattern space between the phase next door **** aforementioned input terminal pads in claim 2.
[Claim 4] Spacing with said subdivision dummy pattern arranged to said input terminal pad and its perimeter in claim 3 is a substrate for electro-optic devices characterized by being set up widely and consisting of spacing of wiring and said dummy pattern of the near.
[Claim 5] It is the substrate for electro-optic devices characterized by for said terminal pad being a junction terminal pad arranged at the method side of the inside of a substrate in claim 1, and setting up widely spacing of said junction terminal pad and said dummy pattern arranged to the perimeter, and consisting of spacing of wiring and said dummy pattern of the near.
[Claim 6] In the pixel field to which the switching element corresponding to each pixel is arranged on a substrate It has the laminating membrane structure to which the laminating of two or more interlayer insulation films and two or more conductive layers was carried out by turns. It is the substrate for electro-optic devices with which flattening of said much more lower layer interlayer insulation film is carried out, and it consists of the conductive layer of the maximum upper layer of these two or more conductive layers by polish processing at least. The substrate for electro-optic devices characterized by having the dummy pattern of the monolayer which consists of said lower layer conductive layer, or a double layer in the seal field formed in the perimeter of said pixel field, and changing from the interlayer insulation film of said polish processing to it.
[Claim 7] In the pixel field to which the switching element corresponding to each pixel is arranged on a substrate It has the laminating membrane structure to which the laminating of two or more interlayer insulation films and two or more conductive layers was carried out by turns. It is the substrate for electro-optic devices with which flattening of said much more lower layer interlayer insulation film is carried out, and it consists of the conductive layer of the maximum upper layer of these two or more conductive layers by polish processing at least. The substrate for electro-optic devices characterized by having the dummy pattern of the monolayer which consists of said lower layer conductive layer, or a

double layer in the periphery field of the outside of the seal field formed in the perimeter of said pixel field, and changing from the interlayer insulation film of said polish processing to it.
[Claim 8] It is the substrate for electro-optic devices characterized by stacking said dummy pattern in claim 6 or claim 7 on the isolated pattern formed in the control wiring layer and this layer of said switching element, being added, and changing.
[Claim 9] In the pixel field to which the switching element corresponding to each pixel is arranged on a substrate It has the laminating membrane structure to which the laminating of two or more interlayer insulation films and two or more conductive layers was carried out by turns. It is the substrate for electro-optic devices with which flattening of said much more lower layer interlayer insulation film is carried out, and it consists of the conductive layer of the maximum upper layer of these two or more conductive layers by polish processing at least. The substrate for electro-optic devices characterized by having the dummy pattern of the monolayer which consists of said lower layer conductive layer, or a double layer in the near field of the actuation circuit which is arranged around said pixel field and supplies a signal to said switching element, and changing from the interlayer insulation film of said polish processing to it.
[Claim 10] In the pixel field to which the switching element corresponding to each pixel is arranged on a substrate It has the laminating membrane structure to which the laminating of two or more interlayer insulation films and two or more conductive layers was carried out by turns. It is the substrate for electro-optic devices with which flattening of said much more lower layer interlayer insulation film is carried out, and it consists of the conductive layer of the maximum upper layer of these two or more conductive layers by polish processing at least. In the corner field of the seal field formed in the perimeter of said pixel field The substrate for electro-optic devices which is low distribution of a consistency and is characterized by having the dummy pattern of the monolayer which consists of said lower layer conductive layer, or a double layer, and consisting of the interlayer insulation film of said polish processing rather than the side field of this seal field, or the boundary region of the corner concerned.
[Claim 11] In the pixel field to which the switching element corresponding to each pixel is arranged on a substrate It has the laminating membrane structure to which the laminating of two or more interlayer insulation films and two or more conductive layers was carried out by turns. It is the substrate for electro-optic devices with which flattening of said much more lower layer interlayer insulation film is carried out, and it consists of the conductive layer of the maximum upper layer of these two or more conductive layers by polish processing at least. The substrate for electro-optic devices characterized by having the dummy pattern of the monolayer which consists of said lower layer conductive layer, or a double layer in the seal field formed in the perimeter of said pixel field, and changing from the interlayer insulation film of said polish processing to it except for the corner field.
[Claim 12] In the pixel field to which the switching element corresponding to each pixel is arranged on a substrate It has the laminating membrane structure to which the laminating of two or more interlayer insulation films and two or more conductive layers was carried out by turns. It is the substrate for electro-optic devices with which flattening of said much more lower layer interlayer insulation film is carried out, and it consists of the conductive layer of the maximum upper layer of these two or more conductive layers by polish processing at least. The substrate for electro-optic devices characterized by having two or more false pixel irregularity patterns containing said lower layer conductive layer, and consisting of the interlayer insulation film of said polish processing in the non-pixel field on said substrate.
[Claim 13] It is the substrate for electro-optic devices characterized by carrying out expansion formation of said false pixel irregularity pattern in claim 15 repeatedly in the two-dimensional direction on said substrate, and changing.
[Claim 14] In claim 12 or claim 13, said 1st conductive layer electrically connected to said switching element and said conductive layer of the upper layer formed on the interlayer insulation film of said

polish processing are connected electrically. Said 2nd conductive layer is included in the medium of said 1st conductive layer and said conductive layer of said upper layer. Said false pixel irregularity pattern The substrate for electro-optic devices characterized by being either of the 2nd dummy pattern which consists of the 1st dummy pattern and said 2nd conductive layer which consists of said 1st conductive layer, or the pile of both.
[Claim 15] It is the substrate for electro-optic devices characterized by for said false pixel irregularity pattern consisting of a false gate line and the false data line at least in claim 17, and changing.
[Claim 16] The electro-optic device characterized by pinching an opto electronics material at spacing of the substrate for electro-optic devices specified in any 1 term of claim 1 thru/or claim 15, and the transparence substrate which counters this, and growing into it.
[Claim 17] Electronic equipment characterized by using for a display the electro-optic device specified to claim 16, and changing.
[Claim 18] The projection mold display characterized by using for a light valve the electro-optic device specified to claim 16, and changing.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the substrate for electro-optic devices which carried out the laminating of the pixel field on the component field for pixel selection about substrates for electro-optic devices, such as a substrate for reflective mold liquid crystal panels.
[0002]
[The technique of relation] Japanese Patent Application No. No. 279388 [eight to] which these people require for the application on October 22, 1996 -- with, the configuration of the substrate for liquid crystal panels described below, a liquid crystal panel, and a projection mold display was indicated. The projection mold indicating equipment (liquid crystal projector) using the reflective mold liquid crystal panel as a light valve it is shown in drawing 1717 -- as -- system optical axis L0 It meets and with the arranged light source section 110, the integrator lens 120, and the polarization lighting system 100 by which an outline configuration is carried out from the polarization sensing element 130 The polarization beam splitter 200 in which S polarization bundle injected from the polarization lighting system 100 is reflected according to S polarization bundle reflector 201, The dichroic mirror 412 which separates the component of blue glow (B) among the light reflected from S polarization bundle reflector 201 of a polarization beam splitter 200, High-reflective-liquid-crystal light valve 300B which modulates the separated blue glow (B), The dichroic mirror 413 which is made to reflect the component of red light (R) among the flux of lights after blue glow was separated by the dichroic mirror 412, and is separated, High-reflective-liquid-crystal light valve 300R which modulates the separated red light (R), High-

reflective-liquid-crystal light valve 300G which modulate the remaining green light (G) which penetrates a dichroic mirror 413, Carry out optical-path reverse of the light modulated with three high-reflective-liquid-crystal light valves 300R, 300G, and 300B, and it compounds by dichroic mirrors 413 and 412 and the polarization beam splitter 200. It consists of projection optical system 500 which consists of a projection lens which projects this synthetic light to a screen 600. The reflective mold liquid crystal panel 30 as shown in the sectional view of drawing 18 , respectively is used for each high-reflective-liquid-crystal light valves 300R, 300G, and 300B.

[0003] The substrate 31 for reflective mold liquid crystal panels which fixed with adhesives on the support substrate 32 with which this reflective mold liquid crystal panel 30 consists of glass or a ceramic, The glass substrate 35 by the side of optical incidence with the counterelectrode (common electrode) 33 which consists of transparence electric conduction film (ITO) which surrounded this substrate 31 top for reflective mold liquid crystal panels in the frame configuration by the sealant 36, set spacing, and carried out opposite arrangement, [in the clearance closed by the sealant 36 between the substrate 31 for reflective mold liquid crystal panels, and a glass substrate 35] It has SH (Super Homeotropic) mold liquid crystal 37 in which a liquid crystal molecule carries out abbreviation vertical orientation in the state of TN (Twisted Nematic) mold liquid crystal of the common knowledge with which it filled up, or no electrical-potential-difference impressing.

[0004] The flat-surface layout which the substrate 31 for reflective mold liquid crystal panels used for this reflective mold liquid crystal panel 30 expanded is shown in drawing 19 . The rectangular pixel field 20 where the pixel electrode 14 of a large number which show the substrate 31 for reflective mold liquid crystal panels to drawing 18 has been arranged in the shape of a matrix (viewing area), The gate line actuation circuits 22R and 22L which are located in the outside of the left right-hand side of the pixel field 20, and scan a gate line (a scan electrode, line electrode) (Y driver), It is located in the outside of the top chord of the pixel electrode 14. The precharge and the test circuit 23 about the data line (a signal electrode, train electrode), The picture signal sampling circuit 24 which is located in the outside of the lower side of the pixel electrode 14, and supplies the picture signal according to image data to the data line, The seal field 27 of a frame configuration where the sealant 37 mentioned above is positioned on the outside of the gate line actuation circuits 22R and 22L, precharge, a test circuit 23, and the picture signal sampling circuit 24, Two or more terminal pads 26 by which are arranged along the bottom edge and fixing connection is made through the anisotropy electric conduction film (ACF) 38 at the flexible tape wiring 39, The data-line actuation circuit 21 which is located between the train of this terminal pad 26, and the seal field 27, and supplies the picture signal according to image data to the data line (X driver), It is located in both the sides of the data-line actuation circuit 21, and consists of junction terminal pads (the so-called fish eye) 29R and 29L for supplying electric power to the counterelectrode 33 of a glass substrate 35.

[0005] In addition, in order to prevent that light carries out incidence also in the circumference circuit (the gate line actuation circuits 22R and 22L, precharge, a test circuit 23, and picture signal sampling circuit 24) located inside the seal field 27, the pixel electrode 14 of the maximum upper layer and the light-shielding film 25 (refer to drawing 18) of this layer are formed in it.

[0006] Drawing 20 is the top view expanding and showing a part of pixel field 20 of the substrate 31 for reflective mold liquid crystal panels, and drawing 21 is the cutting plane showing the condition of having cut along with A-A' in drawing 2020 . Setting to drawing 20 , 1 is P of single crystal silicon. -- It is a mold semi-conductor substrate (N -- a mold semi-conductor substrate may be used), and is the large-sized size of 20mm angle. The P type well field where 2 was formed in the front-face (principal plane) side of a components (MOSFET etc.) formation field among this semi-conductor substrate 1, and 3 are the field oxide (the so-called LOCOS) formed in the isolation in the component agenesis field of the semi-conductor substrate 1. A pixel, such as 768x1024 pixels, is formed as a common well field of the pixel field 20 arranged in the shape of a matrix, and the P type well field 2 shown in drawing 21 is separated with P type well field 2' (refer to drawing 22) of the part which makes the component which

constitutes a circumference circuit (the gate line actuation circuits 22R and 22L, precharge and a test circuit 23, the picture signal sampling circuit 24, and data actuation circuit 21).
[0007] Two openings are formed in the partition field in every pixel at field oxide 3. N+ formed in the front face of the P type well field 2 of the both sides of gate electrode 4a which consists of polish recon or metal silicide formed in the center of the inside of one opening through gate-dielectric-film 4b, and this gate electrode 4a Mold source field 5a and N+ Mold drain field 5b constitutes the N channel mold MOSFET for pixel selection (insulated gate field effect transistor). Each gate electrode 4a of two or more pixels which adjoin a line writing direction extends in the direction of the scanning line (pixel line writing direction), and constitutes the gate line 4.
[0008] Moreover, the P type capacity electrode field 8 common to a line writing direction formed in the front face of the P type well field 2 inside opening of another side and capacity electrode 9a which consists of polish recon or metal silicide formed through insulator layer (dielectric film) 9b on this P type capacity electrode field 8 constitute the retention volume C for holding the signal chosen by MOSFET for pixel selection.
[0009] The 1st interlayer insulation film 6 is formed on gate electrode 4a and capacity electrode 9a, and the 1st metal layer which makes aluminum a subject is formed on this insulator layer 6.
[0010] While carrying out electric conduction contact at drain field 5b through source electrode wiring 7a which projects in the shape of a ctenidium from the data line 7 (refer to drawing 20) which extends in the direction of a train, and the data line 7, and carries out electric conduction contact through contact hole 6a at source field 4b, and contact hole 6b, the junction wiring 10 which carries out electric conduction contact is included in the 1st metal layer through contact hole 6c at capacity electrode 9a.
[0011] The 2nd interlayer insulation film 11 is formed on the 1st metal layer which constitutes the data line 7, source electrode wiring 7a, and the junction wiring 10, and the 2nd metal layer which makes aluminum a subject is formed on this 2nd interlayer insulation film 11. As for this 2nd metal layer, the wrap light-shielding film 12 is contained in the whole surface of the pixel field 20. In addition, the 2nd metal layer which constitutes this light-shielding film 12 constitutes wiring 12b for connection between components (refer to drawing 22) in the circumference circuit (the gate line actuation circuits 22R and 22L, precharge and a test circuit 23, the picture signal sampling circuit 24, and data actuation circuit 21) formed in the perimeter of the pixel field 20.
[0012] Opening 12a for plug penetration has opened in the location corresponding to the junction wiring 10 of a light-shielding film 12. The 3rd interlayer insulation film 13 is formed on a light-shielding film 12, and the pixel electrode 14 as a reflector of the shape of a rectangle corresponding to this 3rd interlayer insulation film 13 top is formed in a part for 1 pixel of abbreviation. The contact hole 16 which penetrates the 3rd and 2nd interlayer insulation film 13 and 11 is formed so that it may be located in the inside corresponding to opening 12a of a light-shielding film 12. the refractory metal layer side deposited on the 3rd interlayer insulation film 13 after embedding refractory metals, such as a tungsten, with a CVD method in this contact hole 16, and the front-face side of the 3rd interlayer insulation film 13 -- CMP (chemical mechanical polishing) -- it deletes by law and flattening is carried out to the mirror plane. Subsequently, an aluminum layer is formed, for example by the low-temperature spatter, and the pixel electrode 14 of the shape of a rectangle whose one side is about 15-20 micrometers is formed by patterning. The junction wiring 10 and the pixel electrode 14 are electrically connected by the column-like connecting plug (current carrying part between layers) 15. And on the pixel electrode 14, the passivation film 17 is formed extensively.
[0013] In addition, as the formation approach of a connecting plug 15, after carrying out flattening of the 3rd interlayer insulation film 13 by the CMP method, opening of the contact hole is carried out and there is also the approach of embedding refractory metals, such as a tungsten, into it.
[0014] The flattening processing by the CMP method for such 3rd interlayer insulation film 13 is an indispensable process for forming Mr. front surface mirror Men's pixel electrode 14 as a reflector formed on it for every pixel. Moreover, it is needed even when forming the dielectric mirror film through a

protective coat on the pixel electrode 14. This CMP method is the technique of grinding chemical etching and mechanical polish using the slurry (abrasive liquid) which consists of a component which combines the wafer in front of a scribe and is made to advance.

[0015] However, as the electrode wiring 7a and 10 and the light-shielding film 12 of MOSFET for pixel selection or retention volume C are formed as a substrate layer and the pixel field 20 shows to drawing 22 In a circumference circuit field (the gate line actuation circuits 22R and 22L, precharge and a test circuit 23, the picture signal sampling circuit 24, and data actuation circuit 21) Electrode wiring 7a of MOSFET for pixel selection and wiring 12b between components are formed as a substrate layer. Furthermore, since lower layer film 6a which consists of the 1st metal layer in the field of a terminal pad 26, and upper film 26b which consists of the 2nd metal layer put and is formed, Immediately after membrane formation of the 3rd interlayer insulation film 13, surface level 13a shown by the dotted line of drawing 22 is rising in the pixel field, the circumference circuit field, and the terminal pad field. If polish processing of the polished surface-ed of the 3rd big interlayer insulation film 13 of this surface relief is carried out by the CMP method, it will become what the surface relief which also shows inevitably polish result level 13b shown as the continuous line of drawing 22 by the dotted line reflected. Especially in the substrate 31 for liquid crystal panels by the artificer of this application which performed such polish processing wholeheartedly according to research, it became clear that flattening of the front face of the 3rd interlayer insulation film 13 on the pixel field 20 is important.

[0016] It considers as the technique which carries out flattening of the 3rd interlayer insulation film 13 on this pixel field 20, and the dummy pattern of a metal layer with which it was isolated for every pixel between the 1st metal layer of junction wiring 10 grade and the 2nd metal layer (light-shielding film) 12 is made to intervene beforehand, bottom raising is carried out, and the structure of suppressing boom hoisting of all the front faces of a light-shielding film 12 is adopted as JP,9-68718,A. However, if a medium metal layer is formed only for bottom raising for such every pixel, the membrane formation process of an interlayer insulation film also must be added. Moreover, ** by which the surface relief of the interlayer insulation film before polish is stopped, and polish time amount required in order for the initial polish rate of CMP processing to become low on the contrary and to carry out flattening of the front face of an interlayer insulation film 13 to the mirror plane become long, and consumption of an abrasive liquid also increases. Therefore, the structure which forms a dummy pattern for every pixel of the pixel field 20 has a demerit on a manufacture process, and causes the manufacturing-cost high.

[0017]

[Problem(s) to be Solved by the Invention] It is a thickness diagram -- thickness distribution of the 3rd interlayer insulation film 13 after the polish in the substrate 31 for liquid crystal panels which performed CMP processing is shown -- after drawing 23 forms the 3rd interlayer insulation film 13 by about 24000A of thickness until the residual film thickness of the 3rd interlayer insulation film 13 of the core of the pixel field 20 becomes about 12000A. Moreover, the graph which puts the plot x mark in drawing 24 in a row shows distribution of the residual film thickness of the seal left part lengthwise direction which meets the a-a' line in drawing 23 . The graph which puts the plot x mark in drawing 25 in a row shows distribution of the residual film thickness of the pixel central lengthwise direction which meets the b-b' line in drawing 23 . The graph which puts the plot x mark in drawing 26 in a row shows distribution of the residual film thickness of the seal top chord longitudinal direction which meets the c-c' line in drawing 23 . The graph which puts the plot x mark in drawing 27 in a row shows distribution of the residual film thickness of the pixel central longitudinal direction which meets the d-d' line in drawing 23 , and the graph which puts the plot x mark in drawing 28 in a row shows distribution of the residual film thickness of the pixel central longitudinal direction which meets the e-e' line in drawing 23 .

[0018] The maximum thickness difference in the pixel field 20 and the seal field 27 has about 6120A, and the surface smoothness covering the whole substrate including the pixel field 20 and the seal field 27 is still inadequate so that drawing 23 - drawing 28 may show. Moreover, while the center section of the vertical side of the perimeter field of a terminal pad 26 or the seal field 27 is in the fault polish condition,

the center section of the left right-hand side of the seal field 27 is in the polish lack condition.
[0019] As shown in drawing 22 , since the spot-like isolated high terminal pad 26 is discretely arranged in the shape of a train, in the field of a terminal pad 26, ******** appears in the part of isolated high 13c covered with the 3rd interlayer insulation film 13. Therefore, since an initial polish rate becomes large rather than the pixel field 20, the field of a terminal pad 26 has the danger that superfluous polish of the field of a terminal pad 26 will be carried out, and a substrate layer (upper film 26b) will be exposed although flattening of the pixel field 20 is not carried out enough yet.
[0020] As a means to cancel the superfluous polish condition in such a terminal pad 26, the approach of depositing the 3rd interlayer insulation film 13 thickly beforehand is mentioned. Since according to this approach flattening of the 3rd interlayer insulation film 13 in this field is mostly completed before a substrate layer is exposed even if polish of the field of a terminal pad 26 advances quickly, even if the polish rate after it falls remarkably compared with an initial polish rate and increases polish time amount for flattening of the pixel field 20, it can prevent exposure of a substrate layer.
[0021] however, the refractory metal which constitutes a connecting plug 15 since the contact hole 16 for a connecting plug 15 becomes rather deep and an aspect ratio becomes large when the 3rd thick interlayer insulation film 13 is formed -- a contact hole 16 -- burying -- hard -- ** -- ** Especially the connecting plug 15 is a current carrying part between jump layers for penetrating the 3rd interlayer insulation film 13 and tying to the pixel electrode 14, after penetrating the 2nd interlayer insulation film 11 and light-shielding film 15, and contact hole 16 self tends to become deep from the first. Moreover, in order for the light which carries out incidence from the clearance between the pixel electrodes 14 to make it hard to advance into components, such as MOSFET, as much as possible through opening 12a, the aperture of a contact hole 16 must also be made thin on the need of making opening 12a as small as possible. For this reason, the aspect ratio of a contact hole 16 becomes large inevitably. So, thin film-ization of the 3rd interlayer insulation film 13 of a ground layer is demanded strongly. However, as mentioned above, in the field of a terminal pad 26, fault polish of the flattening processing by the CMP method of the 3rd interlayer insulation film 13 will actualize.
[0022] On the other hand, since the thickness of the center section of the vertical side of the seal field 27 is dragged by fault polish in the field of a terminal pad 26 and is thin relatively compared with the thickness of the pixel field 20, as shown in drawing 26 and drawing 28 , the center section of the vertical edge of the pixel field 20 or the vertical side of the seal field 27 is in a fault polish condition. Moreover, although near the four-corners section of the left right-hand side of the seal field 27 is dragged by fault polish in the field of a terminal pad 26 and thickness tends to become thin, the initial polish rate has fallen and stopped on the contrary easily being able to grind the center section of the left right-hand side of the seal field 27 on account of the surface smoothness of the seal field 27 before polish. For this reason, as shown in drawing 24 , the center section of the left right margin of heart of the left right-hand side of the seal field 27 or the pixel field 20 is in a polish lack condition. Thus, if the perimeter edge of the pixel field 20 and the seal field 27 have the inclination side, when bringing about decline in the reflective effectiveness of the pixel electrode 14 formed on the 3rd interlayer insulation film 13 after polish, the difficulty of the cel gap adjustment in the case of liquid crystal panel assembly, and the adhesion nonconformity of a sealant and carrying out hole dawn of the contact hole 16 of a connecting plug 15 after CMP processing, optimization of the etching time of a contact hole becomes difficult with a thickness ununiformity.
[0023] An example is taken by the above-mentioned trouble which carried out the antinomy about the interlayer insulation film which requires the polish processing formed between the light-shielding films and pixel electrodes in the substrate for reflective mold liquid crystal panels. Then, the 1st technical problem of this invention In the substrate for electro-optic devices which has the laminating membrane structure which repeated the interlayer insulation film and the conductive layer by turns, and formed membranes on the substrate with which the component field was formed The addition of membrane formation manday is not caused but the interlayer insulation film which should grind the above is also to

offer substrates for electro-optic devices, such as a substrate for liquid crystal panels with the structure which can equalize the polish rate of the interlayer insulation film, without thick-film-izing.
[0024] Moreover, the polished surface of an interlayer insulation film turns into flat Men like a pixel field, and the 2nd technical problem of this invention also has a seal field in offering substrates for electro-optic devices, such as a substrate for liquid crystal panels which can realize improvement in adhesion of improvement in the reflective effectiveness of a pixel electrode, easy-izing of cel gap adjustment, and a sealant, and optimization of the etching time of a contact hole.
[0025]
[Means for Solving the Problem] in order to solve the 1st technical problem of the above , the 1st means which this invention provided do not make the dummy pattern for bottom raising of the interlayer insulation film of the above-mentioned polish processing in the crevice in a pixel field so that it may carry out flattening of the membrane formation surface level of the interlayer insulation film before polish to a whole surface homogeneity as much as possible in a pixel field at least , and be in the point which apply an established wiring layer and be form outside a pixel field at an abbreviation whole surface target . Namely, this invention is set to the pixel field to which the switching element corresponding to each pixel is arranged on a substrate. It has the laminating membrane structure to which the laminating of two or more interlayer insulation films and two or more conductive layers was carried out by turns. It is the substrate for electro-optic devices with which flattening of said much more lower layer interlayer insulation film is carried out, and it consists of the conductive layer of the maximum upper layer of these two or more conductive layers by polish processing at least. It is characterized by having the dummy pattern of the monolayer which consists of said lower layer conductive layer formed in the non-pixel field on said substrate, or a double layer, and consisting of the interlayer insulation film of said polish processing at least near the terminal pad. As a terminal pad, the junction terminal pad arranged rather than the input terminal pad arranged near the substrate edge or it at the method of the inside of a substrate is contained here.
[0026] In the structure which has arranged such a dummy pattern near the terminal pad, since bottom raising of the membrane formation surface level of the interlayer insulation film of polish on a dummy pattern is carried out also near the terminal pad, it is set to the membrane formation surface level and abbreviation equivalent level of an interlayer insulation film of polish processing in a pixel field, and surface level covers the whole and equalizes. Thus, when the polished surface-ed was equalized and CMP (chemical mechanical polishing) etc. is ground, the polish rate near and around a terminal pad field does not become quick at **, but, on the whole, a uniform polish rate is obtained, and the polished surface of the interlayer insulation film of polish processing compares and carries out flattening to old. For this reason, while becoming much more good [flattening of a pixel field] and being able to improve the controllability of the cel gap at the time of the cel assembly using an opposite substrate etc., it becomes easy to determine the etching time of contact holes, such as a current carrying part between layers of the pixel field after polish.
[0027] If uniform flattening of such a polished surface is obtained, thin film-ization of the interlayer insulation film which exposure of the terminal pad layer of a substrate stops being able to happen easily due to fault polish of the terminal pad section, and is applied to polish processing is also realizable. Since the aspect ratio of the contact hole of the current carrying part between layers in a pixel field is improvable with this thin film-ization, it can connect to narrow diameter-ization of opening by narrow diameter-ization of a contact hole. So, the protection-from-light engine performance is improvable.
[0028] In addition, although the current carrying part between this layer connects electrically said 1st conductive layer electrically connected to a switching element, and said conductive layer of the upper layer formed on the interlayer insulation film of said polish processing Said dummy pattern can be considered as either of the 2nd dummy pattern which consists of the 2nd conductive layer which exists in the medium of the 1st dummy pattern which consists of the 1st conductive layer and the 1st conductive layer, and the conductive layer of the upper layers, such as a light-shielding film, or the pile

of both.
[0029] And if the near region of the terminal pad outside a pixel field is also covered with the dummy pattern of a conductive layer, since this dummy pattern will also serve as a light-shielding film, the stray light stops easily being able to go into the component field made from the outside of a pixel field to the substrate, can control a photocurrent, and is useful to an improvement of a switching element property.
[0030] By the way, since it is made to carry out thermocompression bonding of the anisotropy electric conduction film in connection between an input terminal pad and external wiring, said comparatively thin interlayer insulation film after wrap polish is damaged by the conductive particle in a dummy pattern space, and a new fear of causing an input terminal pad and a short circuit usually arises. When the dummy pattern arranged near the input terminal pad carries out abbreviation continuation, is formed in the four-way-type whole surface and grows into it except for the field of cash-drawer wiring, there is a possibility that between the input terminal pads which adjoin through this dummy pattern may short-circuit.
[0031] However, in this invention, the short circuit between adjoining terminal pads can be prevented, equalizing the surface level of the interlayer insulation film immediately after membrane formation which should carry out polish processing, since the dummy pattern arranged around an input terminal pad consists of two or more subdivision dummy patterns subdivided superficially. A short probability becomes smaller, so that the number of subdivision dummy patterns is increased.
[0032] Here, it is desirable between phase next door **** input terminal pads that it is a non-dummy pattern space. The electric conduction line of flexible tape wiring with which pressure strong at the time of thermocompression bonding joins this non-dummy pattern space is adjoined. If the dummy pattern is formed continuously, by the conductive particle in the anisotropy electric conduction film, a terminal pad and a shorting probability are high, and have the danger of causing the short circuit between input terminal pads through a short circuit with a dummy pattern. It considers as a non-dummy pattern space for preventing the high short circuit of such danger certainly.
[0033] It comes to set up spacing of this input terminal pad and the subdivision dummy pattern arranged to that perimeter more widely than spacing of wiring and the dummy pattern of that near. It is for bridge formation with the input terminal pad's and subdivision dummy pattern's by the conductive particle of the anisotropy electric conduction film stopping being able to happen easily, and preventing a short circuit as much as possible.
[0034] Moreover, it comes to set up spacing of a junction terminal pad and the dummy pattern arranged to the perimeter more widely than spacing of wiring and the dummy pattern of the near. Even if a silver paste overflows a junction terminal pad a little, he is trying not to short-circuit as much as possible to the dummy pattern of the near, although a flow is usually achieved with a silver paste on a junction terminal pad.
[0035] In order to solve the 2nd technical problem of the above, the 2nd means of this invention is characterized by having the dummy pattern of the monolayer which consists of a lower layer conductive layer, or a double layer to the seal field formed in the perimeter of not only the near region of a terminal pad but a pixel field, and changing from the interlayer insulation film of said polish processing to it. If the dummy pattern is not laid by the seal field, the interlayer insulation film front face of said polish processing of a pixel field will tend to turn into an inclination side especially in that circumference part, and will invite the difficulty of etching time optimization of the hole by the thickness ununiformity of decline in the reflective effectiveness of the light-shielding film of the conductive layer of the upper layer which should be formed next, and the interlayer insulation film of said polish processing. In order to solve such a problem, it is good to prepare a dummy pattern in a seal field. Since the field near the circumference of a pixel field becomes almost uniform [the surface level of said interlayer insulation film which should carry out polish processing] also including a seal field by this, even if it performs polish processing, it is hard to produce an inclination side and a thickness ununiformity in the interlayer insulation film of the polish processing in a pixel field.

[0036] However, it is the seal field in which the dummy pattern was prepared, and also if the dummy pattern is not prepared outside, the interlayer insulation film on a seal field will become an inclination side by polish processing. In the assembly of an electro-optic device, this causes trouble to control of the gap between substrates at the time of sticking with an opposite substrate (it is also called a cel gap), or produces nonconformity in the adhesion of a sealant.
[0037] In order to solve this, the thing of a seal field for which a dummy pattern is prepared also in an outside periphery field is still more desirable.
[0038] In addition, this dummy pattern can be considered as either of the 2nd dummy pattern which consists of the 2nd conductive layer which exists in the medium of the 1st dummy pattern which consists of the 1st conductive layer electrically connected to a switching element and the 1st conductive layer, and the conductive layer of said upper layers, such as a light-shielding film, or the pile of both.
[0039] Furthermore, as for the dummy pattern prepared in the periphery field of this seal field and a seal field, it is desirable to stack on the pattern isolated in the control wiring layer and this layer of a switching element, and for it to be added, and to change. Moreover, if there is need, also as for the dummy pattern of the near region of a terminal pad, it is desirable to stack on the pattern isolated in the control wiring layer and this layer of switching, and for it to be added, and to change. If this pattern is also used as a base plate for bottom raising, flattening of the surface level of the interlayer insulation film of said polish processing can be adjusted still more minutely.
[0040] And it is characterized by having the dummy pattern of the monolayer which consists of a lower layer conductive layer, or a double layer in the near field of the actuation circuit which is arranged around a pixel field and supplies a signal to a switching element in this invention again, and changing from the interlayer insulation film of said polish processing to it. It is useful to flattening of the interlayer insulation film of said polish processing etc. by forming a dummy pattern in the staging area of a seal field and a pixel field etc. In addition, this dummy pattern can be considered as either of the 2nd dummy pattern which consists of the 1st dummy pattern and said 2nd conductive layer which consists of said 1st conductive layer, or the pile of both.
[0041] Furthermore, in this invention, it is characterized by having the dummy pattern of the monolayer which is low distribution of a consistency and consists of said lower layer conductive layer rather than the interlayer insulation film of said polish processing, or a double layer, and changing rather than the side field of this seal field, or the boundary region of the corner concerned, in the corner field of the seal field formed in the perimeter of a pixel field. In the corner field of a seal field, it is the dispersive set of two or more subdivision dummy patterns instead of a large continuous extension side (so-called solid) like the dummy pattern of the boundary region of seal **** or the corner concerned. For this reason, if the front face of the interlayer insulation film before the polish in the seal four-corners section is presenting the Men granularity which the irregularity by two or more discrete subdivision dummy patterns reflected and polish processing is performed Rather than the case where the four-corners section is formed in respect of continuous extension, an initial polish rate becomes quick, and since it goes on in the polish rate list of the four-corners section with the inclination which carries out abbreviation equalization with the polish rate of the seal field inside, the residual-film-thickness variation of a pixel field and a seal field is controlled.
[0042] moreover, in the seal field formed in the perimeter of a pixel field When it has the dummy pattern of the monolayer which consists of said lower layer conductive layer, or a double layer and consists of the interlayer insulation film of said polish processing except for the corner field, Namely, since the corner fell and the boundary part has started, even when there is no dummy pattern in the four-corners section (pattern consistency zero) (it is square), In early stages of polish, the boundary part will be in a ****** condition, an inclination side is formed, and an inclination side affects a way among a pixel field and a seal field at ****. For this reason, overall flattening of a pixel field and a seal field can be obtained.
[0043] In addition, such a dummy pattern can be considered as either of the 2nd dummy pattern which

consists of the 1st dummy pattern and said 2nd conductive layer which consists of said 1st conductive layer, or the pile of both.
[0044] and in this invention, the dummy pattern of a continuous extension side (so-called solid) is formed in a non-pixel field again -- coming out -- there is nothing and it is characterized by having two or more false pixel irregularity patterns containing said lower layer conductive layer, and consisting of the interlayer insulation film of said polish processing in the non-pixel field on a substrate. Since the surface irregularity pattern of a pixel and the surface irregularity pattern of abbreviation resemblance are formed also in front faces other than the pixel field of the interlayer insulation film before polish processing, as soon as a polish rate spreads abbreviation etc. in every part of a substrate from the first stage with a substrate equipped with such a false pixel irregularity pattern, in a pixel field and a seal field at least, the surface surface smoothness of high degree of accuracy is realizable.
[0045] It is more desirable to carry out expansion formation repeatedly and to give space regularity in the two-dimensional direction on a substrate rather than it arranges two or more false pixel irregularity patterns in non-regulation to a non-pixel field. It is for making it respond to the pixel irregularity pattern having space regularity, such as the shape of a matrix, to the pixel field. The surface surface smoothness in a pixel field and a seal field becomes remarkable.
[0046] Although this false pixel irregularity pattern can be constituted from either of the 2nd dummy pattern which consists of the 1st dummy pattern and said 2nd conductive layer which consists of said 1st conductive layer, or a pile of both, it can raise a false degree further by including the pattern of an interlayer insulation film.
[0047] And as this false pixel irregularity pattern, it is desirable to constitute from a false gate line and the false data line at least. It is a part with the remarkable (typical) irregularity these [whose] are pixels, and is because it participates in the concavo-convex regularity of a pixel field most.
[0048] In addition, assembly **** are suitable for using such an electro-optic device for the display of various electronic equipment for the electro-optic device using the above-mentioned substrate for electro-optic devices. For example, suitable [0049] for the light valve of a projection mold indicating equipment
[Embodiment of the Invention] Next, each operation gestalt of this invention is explained based on an accompanying drawing.
[0050] [Operation gestalt 1] They are the top view showing the example of a layout configuration of the substrate for reflective mold liquid crystal panels of the reflective mold liquid crystal panel which drawing 1 requires for the operation gestalt 1 of this invention, and the cutting plane showing the condition of having cut drawing 2 along with the B-B' line in drawing 1 .
[0051] The substrate 131 for reflective mold liquid crystal panels of this example shown in drawing 1 The rectangular pixel field 20 where the pixel electrode 14 shown in drawing 18 has been arranged in the shape of a matrix like the substrate 31 of drawing 18 and drawing 1919 showing the conventional substrate for liquid crystal panels (viewing area), The gate line actuation circuits 22R and 22L which are located in the outside of the left right-hand side of the pixel field 20, and scan a gate line (a scan electrode, line electrode) (Y driver), It is located in the outside of the top chord of the pixel electrode 14. The precharge and the test circuit 23 about the data line (a signal electrode, train electrode), The picture signal sampling circuit 24 which is located in the outside of the lower side of the pixel electrode 14, and supplies the picture signal according to image data to the data line, The seal field 127 where the sealant 36 (refer to drawing 18) mentioned above in the outside of the picture signal sampling circuit 24 at the gate line actuation circuits 22R and 22L, precharge, and test circuit 23 list is positioned, Two or more input terminal pads 26 by which are arranged along the bottom edge and fixing connection is made through the anisotropy electric conduction film at flexible tape wiring, The data-line actuation circuit 21 which is located between the train of this terminal pad 26, and the lower side of the seal field 127, and supplies a sampling signal to the picture signal sampling circuit 24 (X driver), It is located in both the sides of the data-line actuation circuit 21, and consists of junction terminal pads (the so-called fish eye)

29R and 29L for supplying electric power to the counterelectrode 33 of the glass substrate 35 which shows the amplitude core electrical potential difference of liquid crystal alternating current actuation to drawing 18 from the input terminal pad 26. The gate line actuation circuits 22R and 22L and the data-line actuation circuit 21 have a shift register respectively, and according to the shift data transfer in a shift register, a scan signal is supplied to a gate line and they supply a sampling signal to the picture signal sampling circuit 24 respectively. The signal sampling circuit 24 supplies a picture signal to the data line in response to a sampling signal.

[0052] The seal field 127 of the frame configuration (the shape of a frame) which encloses the pixel field 20 by this example especially is the dummy pattern space of the isolated continuous extension side (so-called solid) as shown by hatching. Moreover, it has a dummy pattern space of a continuous extension side as also shows the perimeter of the input terminal pad 26, the junction terminal pads 29R and 29L, or the data-line actuation circuit 21 by hatching.

[0053] The planar structure and cross-section structure of the pixel field 20 of this panel substrate 131 are the same as the structure shown in drawing 20 and drawing 21 . That is, as shown in drawing 2 , it is P of single crystal silicon at large-sized size (about 20mm angle). -- The P type well field 2 is formed in the front-face (principal plane) side of the mold semi-conductor substrate (N -- a mold semi-conductor substrate may be used) 1, and field oxide (the so-called LOCOS) 3 is formed on it. A pixel, such as 768x1024 pixels, is formed as a common well field of the pixel field 20 arranged in the shape of a matrix, and this P type well field 2 is separated with P type well field 2' of the part which makes the component which constitutes a circumference circuit (the gate line actuation circuits 22R and 22L, precharge and a test circuit 23, the picture signal sampling circuit 24, and data-line actuation circuit 21).

[0054] Gate electrode 4a which consists of polish recon or metal silicide etc. which two openings are formed in the partition field in every pixel of field oxide 3, and was formed in the center of the inside of one opening through gate-dielectric-film 4b, N+ formed in the front face of the P type well field 2 of the both sides of this gate electrode 4a Mold source field 5a and N+ With mold drain field 5b, the N channel mold MOSFET (insulated gate field effect transistor) for a switching element, i.e., pixel selection, is constituted. As shown in drawing 20 , each gate electrode 4a of two or more pixels which adjoin a line writing direction extends in the direction of the scanning line (pixel line writing direction), and constitutes the gate line 4.

[0055] Although not illustrated in drawing 2 The P type capacity electrode field 8 common to a line writing direction formed in the front face of the P type well field 2 inside opening of another side as shown in drawing 21 , MOSFET for pixel selection is minded with maintenance electrode 9a which consists of polish recon or metal silicide formed through insulator layer (dielectric film) 9b on this P type capacity electrode field 8. The retention volume (it is also called storage capacitance) C for holding the picture signal supplied to the pixel electrode 14 is constituted.

[0056] Capacity electrode 9a can use and form the membrane formation process of the polish recon which constitutes gate electrode 4a of MOSFET for pixel selection, or a metal silicide layer here. Moreover, insulator layer (dielectric film) 9b under capacity electrode 9a can also use and form the insulator layer membrane formation process which constitutes gate-dielectric-film 4b. Insulator layers 9b and 4b are about 400-800A thickness by the oxidizing [thermally] method. Capacity electrode 9a and gate electrode 4a are the double layer systems which formed the polish recon layer by the thickness of about 1000-2000A, and put Mo or the silicide layer of a refractory metal like W on the thickness of about 1000-3000A on it. By using the above-mentioned gate electrode 4a as a mask, the source and the drain fields 5a and 5b inject an N type impurity into the substrate front face of the both sides in self align by ion implantation, and are formed in it.

[0057] The P type capacity electrode field 8 can be formed by the doping processing by the ion implantation of dedication, and heat treatment (drive-in), and may perform an ion implantation before a gate electrode formation process. That is, the impurity of the P well 2 and isomorphism is poured in after formation of insulator layer 9b, and rather than the depths, the front face of the P type well 2 is

accomplished to a high high-impurity-concentration field, and forms a low resistive layer. The desirable high impurity concentration of the P type well 2 is 3 1x1017cm. It is the following and about 1x1016 to 5x1016 are desirable. the desirable surface high impurity concentration of the source and the drain fields 5a and 5b -- the desirable surface high impurity concentration of 1x1020-3x1020cm3 and the P type capacity electrode field 8 -- 1x1018-5x1019cm3 it is -- although -- 1x1018-1x1019cm3 from the dependability of insulator layer 9b which constitutes retention volume C, and a pressure-proof viewpoint It is desirable.

[0058] The 1st interlayer insulation film 6 is formed on gate electrode 4a and capacity electrode 9a, and the 1st conductive layer (henceforth the 1st metal layer) which makes aluminum a subject is formed on this insulator layer 6. the shape of a ctenidium from the data line 7 (refer to drawing 20) and the data line 7 which extends in the direction of a train in the 1st metal layer -- projecting -- substance -- source electrode wiring 7a which carries out electric conduction contact through baton hole 6a at source field 4b, and substance -- while carrying out electric-conduction contact through baton hole 6b at drain field 5b -- substance -- the junction wiring 10 which carries out electric-conduction contact is included in capacity electrode 9a through baton hole 6c.

[0059] The 1st interlayer insulation film 6 deposited upwards about 1000A (silicon oxide film formed by the elevated-temperature CVD method) for example, of HTO film here, deposits BPSG (silicate glass film including boron and Lynn) on it by the thickness of about 8000-10000A, and is formed in it. The 1st metal layer which constitutes source electrode wiring 7a and the junction wiring 10 is made into four layer systems by which the laminating was carried out by Ti/TiN/aluminum/TiN from the lower layer.

[0060] As for about 1000A and the layer [3rd] aluminum layer, the TiN layer of about 100-600A and a two-layer eye is made [Ti of the lowest layer] into about 300-600A for thickness, as for the TiN layer of about 4000-10000A and the maximum upper layer.

[0061] The 2nd interlayer insulation film 11 is formed on this 1st metal layer, and the 2nd conductive layer (henceforth the 2nd metal layer) which makes aluminum a subject is formed on this 2nd interlayer insulation film 11. As for this 2nd metal layer, the light-shielding film 12 which shades the spacing section of a bonnet and the adjoining pixel electrode 14 is contained in most pixel fields 20. In addition, the 2nd metal layer which constitutes this light-shielding film 12 is used in the circumference circuit (the gate line actuation circuits 22R and 22L, precharge and a test circuit 23, the picture signal sampling circuit 24, and data-line actuation circuit 21) formed in the perimeter of the pixel field 20 also as wiring 12for connection b between components (refer to drawing 2).

[0062] The 2nd interlayer insulation film 11 deposited upwards about 3000-6000A (the TEOS film is called hereafter) of silicon oxide film which is made from TEOS (tetraethyl orthochromatic silicate), and is formed by the plasma-CVD method, deposits the SOG film (spin-on glass membrane), and after it deletes it here with etchback, further, on it, the 2nd TEOS film is deposited on the thickness of about 2000-5000A, and it is formed in it.

[0063] The 2nd metal layer which constitutes light-shielding film 12 grade is made into four layer systems by which could make it be the same as that of the 1st metal layer, for example, the laminating was carried out by Ti/TiN/aluminum/TiN from the lower layer.

[0064] As for about 1000A and the layer [3rd] aluminum layer, the TiN layer of about 100-600A and a two-layer eye is made [Ti of the lowest layer] into about 300-600A for thickness, as for the TiN layer of about 4000-10000A and the maximum upper layer.

[0065] Opening 12a for plug penetration has opened in the location corresponding to the junction wiring 10 of a light-shielding film 12. The 3rd interlayer insulation film 13 is formed on a light-shielding film 12, and the pixel electrode 14 as a reflector of the shape of a rectangle corresponding to 1 pixel of abbreviation is formed on this 3rd interlayer insulation film 13. The 3rd interlayer insulation film 13 could also be made to be the same as that of the 2nd interlayer insulation film 11, and deposited about 3000-6000A of TEOS film here upwards, and the SOG film is deposited, and after deleting it with etchback, further, on it, the 2nd TEOS film is deposited on the thickness of about 16000-24000A, and it is formed.

Or it is also possible not to deposit the SOG film between TEOS film, but to constitute the 3rd interlayer insulation film only from TEOS film. The thickness at this time has desirable about 16000-24000A. Moreover, you may make it the configuration which raised moisture resistance by forming a silicon nitride film in the bottom of the TEOS film, or forming a silicon nitride film on the TEOS film. In addition, when a silicon nitride film serves as the upper layer, before depositing this silicon nitride film, flattening of the TEOS film will be carried out by the CMP method etc., or flattening of the silicon nitride film itself will be carried out by the CMP method etc.

[0066] The contact hole 16 which penetrates the 3rd and 2nd interlayer insulation film 13 and 11 is formed so that it may be located in the inside corresponding to opening 12a of a light-shielding film 12. the refractory metal layer side deposited on the 3rd interlayer insulation film 13 after embedding refractory metals, such as a tungsten, with a CVD method in this contact hole 16, and the front-face side of the 3rd interlayer insulation film 13 -- CMP (chemical mechanical polishing) -- it deletes by law and flattening is carried out to the mirror plane. The remaining thickness of the interlayer insulation film 13 at this time adjusts the amount of polishes so that it may become about 4000-10000A in the thinnest part.

[0067] Subsequently, an aluminum layer is formed in thickness of about 300-5000A, for example by the low-temperature spatter, and the pixel electrode 14 of the shape of a rectangle whose one side is about 15-20 micrometers is formed by patterning. The connecting plug (current carrying part between layers) 15 of a refractory metal jumps over a part for one layer of metal layers of a light-shielding film 12, and is making it flow through the junction wiring 10 and the pixel electrode 14. In addition, as the formation approach of a connecting plug 15, after carrying out flattening of the 3rd interlayer insulation film 13 by the CMP method, opening of the contact hole is carried out and there is also the approach of embedding refractory metals, such as a tungsten, into it. Moreover, opening 12a of the 2nd metal layer 12 is enlarged, the 2nd junction wiring which consists of the 2nd metal layer 12 in this opening 12a is formed for example, in the shape of a rectangle, the 1st junction wiring 10 and this 2nd junction wiring are connected, and you may make it connect the 2nd junction wiring and pixel electrode 14 through a connecting plug 15. And on the pixel electrode 14, the passivation film 17, such as silicon oxide with a thickness of about 500-2000A, is formed extensively. In addition, on the passivation film 17, in case a liquid crystal panel is constituted, the orientation film is formed in the whole surface, and rubbing processing is performed. In this example, although the pixel electrode 14 is formed of the 3rd conductive layer (henceforth the 3rd metal layer), when carrying out substrate formation of the metal layer in the process which can be multilayered more, you may form in the upper layer more. Anyway, the pixel electrode 14 is formed in the maximum upper layer of two or more metal layers.

[0068] In addition, although the silicon oxide film is used as mentioned above considering the pixel field 20 as wrap passivation film 17, in a circumference circuit field, a seal field, and the scribe section, a silicon nitride film with a thickness of about 2000-10000A is used. The dielectric mirror film may be formed on the passivation film 17.

[0069] As shown in drawing 1 , around the pixel field 20 which occupies most rectangular semi-conductor substrates 1, the seal field 127 encloses in the shape of a frame. Although this seal field 127 is a border area with the non-pixel field (a circumference circuit field, a terminal pad field, scribe field) where the pixel field 20 and liquid crystal are not enclosed, in this example, a part of circumference circuit (the gate line actuation circuits 22R and 22L, precharge and a test circuit 23, picture signal sampling circuit 24) is included in the seal field 127, and only the data-line actuation circuit 21 is arranged on the outside of the seal field 127. In addition, it is not necessary to say that the data-line actuation circuit 21 may be arranged inside the seal field 127.

[0070] And as the cross-section structure of the seal field 127 of this example is shown in drawing 2 , the upper dummy pattern B of the isolated continuous extension side set to gate electrode 4a from the isolated lower layer dummy pattern A of a continuous extension side and the 2nd isolated metal layer which consist of pattern 127a of the continuous extension side which consists of the isolated polish

recon or metal silicide etc., and the 1st metal layer on field oxide 3 is contained. Pattern 127a can use and form the formation process of gate electrode 4a. Moreover, the dummy patterns A and B can also be formed by process use in the 1st metal layer and the 2nd metal layer. Immediately after membrane formation of the 3rd interlayer insulation film 13, bottom raising only of the part of the thickness of these pattern 127a and the dummy patterns A and B is carried out uniformly, and the surface level has come to spread abbreviation etc. on the surface level of a pixel field or a circumference circuit field for it.

[0071] Not to mention the perimeter of the data-line actuation circuit 21 allotted to the outside of the seal field 127, as hatching of drawing 4 - drawing 6 , and drawing 9 R> 9 shows, the perimeter of the field of the junction terminal pads 29R and 29L or the input terminal pad 26 serves as a dummy pattern space electrically clamped by floating or supply voltage except for the wiring field. Namely, although it has structure which accumulated upper 26b which consists of lower layer 26a and the 2nd metal layer which the input terminal pad 26 of this example also becomes from the 1st metal layer The lower layer dummy pattern A of the isolated continuous extension side which consists of the 1st metal layer formed on the 1st interlayer insulation film 6 on field oxide 3 in the cross-section structure of a dummy pattern space The upper dummy pattern B of the isolated continuous extension side which consists of the 2nd metal layer formed on the 2nd interlayer insulation film 11 is contained. These dummy patterns A and B can also be formed by process use of a metal layer. And immediately after membrane formation of the 3rd interlayer insulation film 13, the surface level stacks only the part of the thickness of these dummy patterns A and B, it is added, and since [the] it stacks and the help effectiveness will be reflected to a field soon, the surface level of a pixel field or a circumference circuit field, abbreviation, etc. have come to spread the level of a right above [the input terminal pad 26] part.

[0072] Moreover, two or more wiring LOUT which prolonged and came out from the data-line actuation circuit 21 also in the Hasama field X between the bottom side of the seal field 127, and the data-line actuation circuit 21 as shown in drawing 4 and drawing 5 It is covered with the dummy pattern M between wiring of isolated length length in between. This dummy pattern M between wiring applies a metal layer, and is formed.

[0073] However, since the method of forming the input terminal pad 26 embeds upper 26b at big opening opened in the 2nd interlayer insulation film 11 on lower layer 26a and a big central hollow is formed in upper 26b, a hollow will be inevitably formed also in the 3rd interlayer insulation film 13 of the right above. As mentioned above in membrane formation of the 3rd interlayer insulation film 13, when formation of the SOG film is included, the hollow of upper 26b can be made to some extent shallow.

[0074] However, the occupancy area of the input terminal pad 26 is compared with the contact hole of a wiring electrode, and since it is large-scale, it cannot cancel enough the hollow of the 3rd interlayer insulation film 13 of terminal pad 26 right above only by the addition of the formation process of the SOG film.

[0075] Drawing 3 is the sectional view showing another structure of an input terminal pad. In drawing 3 , after opening two or more narrow diameter contact holes on lower layer 26a, upper 26b' is embedded and terminal pad 26' is formed. With this structure, since the amount of depression of the ingredient of upper 26b' into a contact hole decreases and a detailed hollow distributes, flattening of the upper 26b' front face is carried out. For this reason, it is [flattening-] easy to make a hollow hard to reflect in the front face which formed the 3rd interlayer insulation film 13 on it.

[0076] Thus, by this example, in almost all the fields of the exterior of a pixel field or a circumference circuit field, since the dummy pattern space (dummy patterns A and B) of a continuous extension side puts and is formed so that a pattern consistency may approach to 100%, also immediately after membrane formation of the 3rd interlayer insulation film 13, the surface level continues all over a substrate, and turns into abbreviation uniform level. So, if CMP polish processing is performed after this, the polished surface of the 3rd interlayer insulation film 13 will be set to the level shown as the continuous line of drawing 2 or drawing 3 . Since the front face of the 3rd interlayer insulation film 13

before polish does not serve as especially the isolated high one in the field of the input terminal pad 26 and 26', in the field, an initial polish rate is not too quick, it is hard to expose the input terminal pad 26 and 26', and a polish rate equalizes. For this reason, it becomes possible to increase the CMP polish processing time of polishes, i.e., the amount, rather than the amount (about 4000A) of old. Thus, the profit which can equalize a polish rate brings about after all that thickness of the 3rd interlayer insulation film 13 after polish can be made thin. And since the aspect ratio of the open beam contact hole 16 can be improved to opening 12a of the light-shielding film 12 of the pixel field 20 and it contributes to narrow diameter-ization of a connecting plug 15, the opening area of opening 12a can be reduced and the protection-from-light engine performance can be raised. Moreover, the profit which can increase the amount of polishes is connected with the profit which can ease a level difference by CMP polish, without forming the SOG film, even if the level difference of opening 12a produced when the 3rd interlayer insulation film 13 consists only of TEOS film is deep. Therefore, the membrane formation process of the 3rd interlayer insulation film 13 can be simplified, and it ** to improvement in productivity.

[0077] It is covered with the flat-surface layout of the dummy pattern space of this example all over abbreviation, without leaving except for data-line actuation circuit 21, signal wiring, power-source wiring, input terminal pad 26, and junction terminal pad 29R.29L among the outsides of the seal field 127, as hatching of drawing 1 shows. It is Wiring LOUT as shown in the Hasama field X of the data-line actuation circuit (it consists of a shift register and the logical circuit which generates a sampling signal based on the output) 21, and the seal field 127 at drawing 4 or drawing 5 . It is covered with the dummy pattern M between wiring of the isolated length length formed in between, the dummy pattern NR by the side of the left right end of a substrate, and NL. Wiring LOUT Spacing with the dummy pattern M between wiring is about 5 micrometers. Output wiring LOUT which outputs a sampling signal to the picture signal sampling circuit 24 from the data-line actuation circuit (a shift register and logical circuit) 21 It extends, and since it has come out, it is regularly covered with the dummy pattern M between wiring. Moreover, wiring which goes to a way among substrates from the field of the input terminal pad 26 as shown in drawing 6 The wiring LIN inputted into the data-line actuation circuit 21 (DXIN (data signal), power sources Vddx and Vssx, a clock signal, reversal clock signal, etc.), Since it can divide roughly into wiring (DYIN (data signal), power sources Vddy and Vssy, a clock signal, reversal clock signal, etc.) inputted into the gate line actuation circuits 22R and 22L, precharge, and a test circuit 23, The way separates to the wiring LIN which should input into the data-line actuation circuit 21 each wiring L once pulled out in the direction of a train (graphic display lengthwise direction) from the input terminal pad 26 in the halfway line writing direction wiring field (graphic display longitudinal direction) W, and the other wiring. For this reason, two or more subdivision dummy pattern S1 -S3 of the isolated rectangle formed in the Hasama field Y of the field of the input terminal pad 26, and the data-line actuation circuit 21 between the input terminal pad 26 and input wiring from there It is covered with the dummy pattern T between wiring of the isolated rectangle formed between the wiring LIN inputted into the data-line actuation circuit 21. In addition, in drawing 6 , the input terminal pad 26 reduces the number, and is illustrated.

[0078] the right and left from there [the rectangle-like electric conduction contact section 261 and there] where the flat-surface configuration of the input terminal pad 26 occupies the whole abbreviation -- which side -- bringing near -- the method of the inside of a substrate (the direction of a train) -- the shape of a narrow width -- flare appearance -- it consists of the wiring cash-drawer section 262 the bottom. The wiring cash-drawer section 262 of the input terminal pad 26 which the wiring cash-drawer section 262 of the input terminal pad 26 located in right-hand side from right-and-left Chuo Line of a substrate is brought near and located in the left-hand side of the electric conduction contact section 261, and is located in left-hand side from right-and-left Chuo Line of a substrate is brought near and located in the right-hand side of the electric conduction contact section 261. Between the wiring cash-drawer sections 262, it is the subdivision dummy pattern S2 of isolated horizontal length. It is arranged. Furthermore, between the wiring L pulled out from there between the point sections of

the wiring cash-drawer section 262, it is the subdivision dummy pattern S3 of an isolated rectangle. It is straddled and formed. And in the substrate edge of the input terminal pad 26, it is the subdivision dummy pattern S1 of an isolated rectangle again. It is arranged.

[0079] The dummy pattern NR by the side of the left right end of the substrate mentioned above, and NL It is reached and formed to the location of the input terminal pad 26, and isolated subdivision dummy pattern S2 ' is arranged at the free area between the wiring cash-drawer sections 262 of the input terminal pad 26 of the maximum outside on either side. Moreover, the dummy pattern NR and NL A head is the dummy pattern NR and NL, although it has gathered at the head of the input terminal pad 26. Subdivision dummy pattern S0 isolated in the substrate marginal corner by the side of a head It is arranged. In addition, the flat-surface configuration of a subdivision dummy pattern can choose not only a rectangle (a square, rectangle) but various configurations (a triangle, a polygon, curvilinear form, etc.). For example, it may cover with a hexagon (forward hexagon)-like subdivision dummy pattern in the shape of [of a bee] a blow hole, and it may be arranged.

[0080] Two or more input terminal pads 26 are connected to the flexible tape wiring 39 by thermocompression bonding through the anisotropy electric conduction film (ACF) 38, as shown in drawing 18 . The broken line of drawing 6 shows the edge of the field which the anisotropy electric conduction film 38 occupies. The flexible tape wiring 39 consists of insulating flexible tape 39a and electric conduction line 39b of the shape of two or more stripe put on this, as shown in drawing 7 and drawing 8 . The anisotropy electric conduction film 38 is inserted between the edge of this flexible tape 39a, and the train of the input terminal pad 26.

[0081] The anisotropy electric conduction film 38 consists of conductive particle 38a with a particle size of about 5-10 micrometers and insulating resin material 38for adhesion b. Flexible tape 39a is stuck by pressure until the thickness is crushed by about 2-10 micrometers. Since it connects conductively through conductive particle 38a which is crushed and is distributed discretely, as for a terminal pad 26 and electric conduction line 39b of the flexible tape wiring 39, the anisotropy electric conduction film 38 has conductivity only in the thickness direction. In addition, drawing 7 and drawing 8 also reduce the number, and the input terminal pad 26 is illustrated.

[0082] Since the surface level of the 3rd interlayer insulation film 13 immediately after the membrane formation on the input terminal pad 26 will become it of the pixel field 20 instead of the isolated high one, and an abbreviation EQC as mentioned above if a dummy pattern space (dummy patterns A and B) is stacked and added to the perimeter of the input terminal pad 26, while an initial polish rate falls and being able to prevent polish of input terminal pad 26 self also in the field of the input terminal pad 26, at a polish process, thin film-ization of the 3rd interlayer insulation film 13 is realizable. Here, if the dummy pattern space is formed in the perimeter of each input terminal pad 26 at the continuation whole surface, when carrying out thermocompression bonding of the anisotropy electric conduction film 38, there is a possibility that between the input terminal pads 26 may short-circuit through conductive particle 38a and a dummy pattern.

[0083] However, in this example, a dummy pattern is not prepared between the input terminal pads 26, but it has become non-dummy pattern space E, and the perimeter of the input terminal pad 26 is subdivision dummy pattern S1 -S3. It is covered. For this reason, the short circuit between the input terminal pads 26 can be prevented. The input terminal pad 26 and subdivision dummy pattern S0 -S3 Spacing and subdivision dummy pattern S0 -S3 Spacing of a between is Wiring L and dummy pattern S4. It is set up more widely than spacing (about 5 micrometers). It is for preventing the short circuit through the anisotropy electric conduction film 38.

[0084] In addition, in order to reduce further the isolated high one of the 3rd interlayer insulation film 13 immediately after membrane formation in the field of the input terminal pad 26, a dummy pattern may be formed between the input terminal pads 26, and the dummy pattern formed between the input terminal pads 26 also uses the short circuit between the input terminal pads 26 as a subdivision dummy pattern at a ****** sake. A short probability becomes smaller, so that the number of subdivisions of a

subdivision dummy pattern is increased. However, the more the number of subdivisions increases, in order that boom hoisting may actualize the more on the front face of the 3rd interlayer insulation film 13 immediately after the membrane formation on a dummy pattern space, it is desirable to select a moderate number. The flat-surface configuration of a subdivision dummy pattern can choose not only a rectangle (a square, rectangle) but various configurations (a triangle, a polygon, curvilinear form, etc.). For example, it may cover with a hexagon (forward hexagon)-like subdivision dummy pattern in the shape of [of a bee] a blow hole, and it may be arranged.

[0085] Drawing 9 is the part plan showing the circumference of junction terminal pad 29R. Junction terminal pad 29R (29L) is the rectangle pad which led to Wiring (supply wiring of the potential used as the criteria of the polarity reversals of the liquid crystal applied voltage in alternating current actuation of liquid crystal) L from the terminal pad 26 of the maximum outside by the side of the data-line actuation circuit 21, sticks a silver paste and is connected conductively to the counterelectrode 33 of a glass substrate 35. In the perimeter of this junction terminal pad 29R (29L), they are the dummy pattern NR and NL. It is formed. For this reason, also in junction terminal pad 29R (29L), the surface level of the 3rd interlayer insulation film 13 immediately after membrane formation can be equalized like a terminal pad 26. "

At this example, they are junction terminal pad 29R and the dummy pattern NR. Spacing is set as 70 micrometers, and even if the flash at the time of making a silver paste adhere happens somewhat, it is set as spacing which cannot short-circuit easily. Namely, junction terminal pad 29R and the dummy pattern NR Spacing is set up more widely than spacing of wiring and the dummy pattern of the near. In addition, the dummy pattern of the perimeter of junction terminal pad 29R is also good also as a subdivision dummy pattern.

[0086] It is a thickness diagram -- thickness distribution of the 3rd interlayer insulation film 13 after the polish in the substrate 131 for liquid crystal panels which performed CMP processing is shown -- after drawing 10 forms the 3rd interlayer insulation film 13 by about 24000A of thickness in the operation gestalt 1 until the residual film thickness of the 3rd interlayer insulation film 13 of the core of the pixel field 20 becomes about 12000A. Moreover, the graph which puts the plot ** mark in drawing 24 in a row shows distribution of the residual film thickness of the seal left part lengthwise direction which meets the a-a' line in drawing 10 . The graph which puts the plot ** mark in drawing 25 in a row shows distribution of the residual film thickness of the pixel central lengthwise direction which meets the b-b' line in drawing 10 . The graph which puts the plot ** mark in drawing 26 in a row shows distribution of the residual film thickness of the seal top chord longitudinal direction which meets the c-c' line in drawing 10 . The graph which puts the plot ** mark in drawing 27 in a row shows distribution of the residual film thickness of the pixel central longitudinal direction which meets the d-d' line in drawing 10 , and the graph which puts the plot ** mark in drawing 28 in a row shows distribution of the residual film thickness of the pixel central longitudinal direction which meets the e-e' line in drawing 10 .

[0087] As shown in these drawings, the maximum thickness difference in the pixel field 20 and the seal field 127 is about 2720A, and spacing (1000A of thickness differences) of an isopachous line compares it with it of drawing 23 , and it is fairly large. The surface smoothness of the pixel field 20 is improved more than twice.

[0088] The maximum thickness difference in the whole substrate (chip) is controlled by about 2910A. The inclination with the low center section of the top chord of the seal field 127 decreases to 1/2 or less abbreviation, and the inclination with the low center section of the lower side of the seal field 127 is decreasing to 1/4 or less abbreviation. Furthermore, the left right-hand side of the seal field 127 has the thinnest top corner, inclination with a high center section is canceled, and inclination is decreasing to 1/4 or less abbreviation. Such a remarkable improvement is because it is covered with the dummy pattern space (dummy patterns A and B) of a continuous extension side (solid) in almost all the fields of the exterior of the pixel field 20 or a circumference circuit field.

[0089] However, to suppress the maximum thickness difference of the pixel field 20 to 1000A or less is

desired. The pixel central vertical line is the valley line of thickness, and the thickness of the center section in the field of the input terminal pad 26 has become thickness distribution of the pixel field 20 with the maximum thickness (about 14500A). This is considered that input terminal Bud's 26 field became the lack of polish conversely with the conventional example of drawing 23 .

[0090] [Operation gestalt 2] They are the part plan showing the neighborhood of the four-corners section of a seal field in the substrate for reflective mold liquid crystal panels which drawing 11 requires for the operation gestalt 2 of this invention, and the sectional view showing the condition of having cut drawing 12 along with the C-C' line in drawing 11 . In addition, in drawing 11 , the field of a dispersion pattern carried out the 1st metal layer, the hatching field of a uniform slash carried out the table of the 2nd metal layer, respectively, and the 3rd metal layer was not illustrated. Moreover, the configuration of those other than the content explained below is the same as that of the substrate for reflective mold liquid crystal panels concerning the operation gestalt 1.

[0091] It has the configuration as the substrate 131 for reflective mold liquid crystal panels of the operation gestalt 1, and abbreviation also with the same substrate 231 for reflective mold liquid crystal panels of this example. While the seal field 127 which encloses the pixel field 20 is the dummy pattern space (the dummy pattern A of the 1st metal layer, and the dummy pattern B of the 2nd metal layer) of the isolated continuous extension side (so-called solid) The perimeter of the input terminal pad 26, the junction terminal pads 29R and 29L, or the data-line actuation circuit 21 also serves as a dummy pattern space (the dummy pattern A of the 1st metal layer, and the dummy pattern B of the 2nd metal layer) of a continuous extension side. For a different point from the dummy pattern formation mode of the operation gestalt 1, in the rectangle field of seal four-corners section 127C of the seal field 127, the dummy pattern of the 1st metal layer is the wiring LOUT of the seal side section. It is the dispersive set of two or more subdivision dummy patterns a instead of a large continuous extension side (so-called solid) like the dummy pattern A with which it covered in between. That is, two or more subdivision dummy patterns a with which the area of the shape of a rectangle or a strip of paper differs set spacing, arrange in the direction in every direction, respectively, and it is dispersively covered with them, and they have 50% or less of pattern consistency. Although the area of two or more subdivision dummy patterns a differs, respectively, they is wholly smaller than the area of the input terminal pad 26. Dummy pattern B' of the 2nd metal layer in seal four-corners section 127C is a rectangle-like continuous extension side. For this reason, the front face of the 3rd interlayer insulation film 13 before the polish in seal four-corners section 127C is presenting the Men granularity which the irregularity by two or more discrete subdivision dummy patterns a reflected as the dotted line of drawing 12 showed.

[0092] In the substrate which formed the subdivision dummy pattern a of low distribution of a consistency in seal four-corners section 127C If CMP processing of the front face of the 3rd interlayer insulation film 13 is carried out, since it will compare with boom hoisting near the flatness of the side section of the seal field 127 and the initial polish rate of four-corners section 127C will become quick, Since it goes on with the inclination in which the seal field 127 surrounded by four parts of four-corners section 127a by the form dragged by this and the polish rate of the inside field carry out abbreviation equalization, the residual-film-thickness variation of the pixel field 20 and the seal field 127 is controlled. It can be said that especially the meaning that gave whenever [granularity] beforehand to the left right corner section of the lower side of the seal field 127 also among seal four-corners section 127a of four parts is large.

[0093] Here, abbreviation etc. spreads and carries out island-like area of two or more subdivision dummy patterns a which can be set to seal four-corners section 127C, and since between the dummy patterns a is vacant as for the equal dispersive thing for which it is, and it carries out, and it assumes that it is distributed at random and a pattern consistency (rate that total of the area of a dummy pattern occupies in an unit area) is made low, the subdivision dummy pattern a is distributed coarsely. For this reason, the initial polish rate of the 3rd interlayer insulation film 13 becomes quick compared with the circumference of seal four-corners section 127C, the boundary part of seal four-corners

section 127C tends to serve as an inclination side quickly, and this inclination side is ground by **** and affects the method of inside. If the number of the subdivision dummy patterns a is reduced and area is enlarged when a pattern consistency is the same, an isolated high inclination will become strong and an initial polish rate will become quick. For this reason, the boundary part of seal four-corners section 127C tends to serve as an inclination side quickly, and this inclination side is ground by the above and the EQC at ****, and affects the method of inside at them. In this example, it is dragged by the residual film thickness of criteria slack seal four-corners section 127C, and becomes easy to double the residual film thickness in the side section of the seal field 127 and the pixel field 20 which were surrounded by seal four-corners section 127C of four parts by adopting the dummy pattern distribution which raises the initial polish rate of seal four-corners section 127C rather than the perimeter. Flat control-ization of the seal field 127 and the pixel field 20 is realized.

[0094] As shown in drawing 11 , in seal four-corners section 127C, two or more strip-of-paper-like subdivision dummy patterns a which carried out the discrete array adjoin the left right-hand side of the seal side in the lengthwise direction, and two or more strip-of-paper-like subdivision dummy patterns a which carried out the discrete array adjoin the longitudinal direction the vertical side of the seal side. It is thought that existence of the strip-of-paper-like subdivision dummy pattern a of a lengthwise direction contributes to flattening of the direction of the seal vertical side since the initial polish rate is the quickest at a part for the long side (lengthwise direction part), and existence of the lateral strip-of-paper-like subdivision dummy pattern a contributes to flattening of the direction of the seal left right-hand side since the initial polish rate is the quickest at a part for the long side (longitudinal direction part). While the strip-of-paper-like subdivision dummy pattern a of a lengthwise direction adjoins the seal vertical side, the lateral strip-of-paper-like subdivision dummy pattern a does not adjoin the seal left right-hand side. In this example Since the strip-of-paper-like subdivision dummy pattern a of a lengthwise direction adjoins the seal left right-hand side and the lateral strip-of-paper-like subdivision dummy pattern a adjoins the seal vertical side, The initial polish rate of the lengthwise direction within seal four-corners section 127C and a longitudinal direction is each other interwoven with, and it is thought that the initial polish rate in this part becomes quick as a result. In addition, it is thought by changing various the configurations, arrays, and pattern consistencies of the subdivision dummy pattern a that the seal field 127 and flattening of the inside field can improve further.

[0095] Moreover, since the corner fell compared with the perimeter, and became hollow-like and the boundary part have start even when there be no dummy pattern in seal four corners section 127C (pattern consistency zero), in early stages of polish, the boundary part will be in a ****** condition, an inclination side be form, and the inclination side affect a way among a pixel field and a seal field at ****. For this reason, overall flattening of the pixel field 20 and the seal field 127 can be obtained.

[0096] It is a thickness diagram -- thickness distribution of the 3rd interlayer insulation film 13 after the polish in the substrate 231 for liquid crystal panels which performed CMP processing is shown -- after drawing 13 forms the 3rd interlayer insulation film 13 by about 24000A of thickness in the operation gestalt 2 until the residual film thickness of the 3rd interlayer insulation film 13 of the core of the pixel field 20 becomes about 12000A. Moreover, the graph which puts the plot ** mark in drawing 24 in a row shows distribution of the residual film thickness of the seal left part lengthwise direction which meets the a-a' line in drawing 13 . The graph which puts the plot ** mark in drawing 25 in a row shows distribution of the residual film thickness of the pixel central lengthwise direction which meets the b-b' line in drawing 13 . The graph which puts the plot ** mark in drawing 26 in a row shows distribution of the residual film thickness of the seal top chord longitudinal direction which meets the c-c' line in drawing 13 . The graph which puts the plot ** mark in drawing 27 in a row shows distribution of the residual film thickness of the pixel central longitudinal direction which meets the d-d' line in drawing 13 , and the graph which puts the plot ** mark in drawing 28 in a row shows distribution of the residual film thickness of the pixel central longitudinal direction which meets the e-e' line in drawing 13 .

[0097] As shown in these drawings, the maximum thickness difference in the pixel field 20 and the seal

field 127 is about 1380A, and spacing (1000A of thickness differences) of an isopachous line compares it with it of drawing 10 , and it is further slow. It compares with the operation gestalt 1 and the surface smoothness of the pixel field 20 is improved more than twice in this example. Although the maximum thickness difference in the whole substrate (chip) is about 2500A, this is because a dummy pattern is a continuous extension side in the field of the input terminal pad 26, so polish is insufficient and thickness is thick still more. The center section of the top chord of the seal field 127 also compares low inclination with the operation gestalt 1, and it decreases in number and requires it for 1/2 or less abbreviation. Moreover, the left right-hand side of the seal field 127 is abbreviation flatness. This is having made low the pattern consistency of the dummy pattern a of the left right corner section of the lower side of the seal field 127, and is because it becomes easy to grind.

[0098] However, the surrounding thickness of the left right corner section of the lower side of the seal field 127 is still thick, and the maximum thickness difference in the pixel field 20 and the seal field 127 has not become in 100A or less so that he can understand from drawing 13 . Although flattening of the pixel field 20 inside is carried out more when the dummy pattern a of four-corners section 127C is completely lost (pattern consistency zero), the boundary part of four-corners section 127C has a possibility of becoming a steep slope. The dummy pattern a which a pattern consistency dwindles is formed as it goes to the upper part of the left right-hand side from left right corner section 127C of the lower side, or the dummy pattern a which a pattern consistency dwindles may be formed as it goes to the center of the lower side from left right corner section 127C of the lower side. In this case, the further flattening of both the fields of the pixel field 20 and the seal field 127 is realizable.

[0099] [Operation gestalt 3] They are the part plan showing the neighborhood of the four-corners section of a seal field in the substrate for reflective mold liquid crystal panels which drawing 14 requires for the operation gestalt 3 of this invention, and the sectional view showing the condition of having cut drawing 15 along with the C-C' line in drawing 14 . In addition, in drawing 14 , the field of a dispersion pattern carried out the 1st metal layer, the hatching field of a uniform slash carried out the table of the 2nd metal layer, respectively, and the 3rd metal layer was not illustrated. Moreover, the configuration of those other than the content explained below is the same as that of the substrate for reflective mold liquid crystal panels concerning the operation gestalt 1.

[0100] The substrate 331 for reflective mold liquid crystal panels of this example has the false pixel irregularity pattern P as a dummy pattern with which it was covered in the shape of a matrix (the shape of a two-dimensional period) in the seal field 227 which encloses the pixel field 20, and its outside field. Without leaving also the data-line actuation circuit 21, the perimeter of the junction terminal pads 29R and 29L, and around the input terminal pad 26, an expansion escape is carried out in the direction in every direction, and this false pixel irregularity pattern P is formed in it. This false pixel irregularity pattern P is for imitating the volume of the component of the pixel which constitutes the pixel field 20, and acquiring the concavo-convex configuration pattern of a pixel front face and resemblance on the front face of the 3rd interlayer insulation film 13.

[0101] false gate line 4p of the 1st metal layer of the **** line breadth likened with the gate line 4 of the lowest layer wiring of a pixel as a component of the false pixel irregularity pattern P in this example false data-line 7p of the 1st metal layer of the **** line breadth assumed as the data line 7 of the 1st metal layer of a pixel, source electrode wiring 7a, and the junction wiring 10, and false source electrode wiring 7ap And false junction wiring 10p False light-shielding film 12p of the 2nd metal layer of the continuous extension side (so-called solid) assumed as the light-shielding film 12 of the 2nd metal layer of a pixel part It exists. For the pattern consistency which consists of lowest layer wiring and the 1st metal layer in each pixel, the pattern consistency which consists of the 1st metal layer in the false pixel irregularity pattern P and the 2nd metal layer since it is about 25% is also abbreviation doubling ****** to it.

[0102] the up-and-down seal field (side section) 237 and Hasama field X' -- setting -- the pixel signal sampling circuit 24 from the data-line actuation circuit 21 -- signal wiring LOUT of the 1st metal layer

as it is -- false data-line 7p ****** -- it is used. For this reason, false gate line 4p ' of the 1st metal layer and false source electrode wiring 7ap ' are false data-line 7p. It does not connect.

[0103] Although it is repeatedly developed in the in-every-direction two-dimensional direction of a substrate and the false pixel irregularity pattern P is formed in it, in this example, the matrix of the false pixel irregularity pattern P contradicts the matrix of the pixel field 20 a little. The component layouts and signal wiring LOUT of a circumference circuit field, such as the data-line actuation circuit 21, the pixel signal sampling circuit 24, and the gate line actuation circuits 22R and 22L By carrying out the design change of the layout, the matrix of the false pixel irregularity pattern P and the matrix of the pixel field 20 can be arranged.

[0104] Since the surface irregularity pattern of a pixel and the surface irregularity pattern of almost resemblance have spread on the space period target, as soon as a polish rate spreads abbreviation etc. also on front faces other than pixel field 20 of the 3rd interlayer insulation film 13 before CMP processing also in the part of substrate 331 throat from the first stage with the substrate 331 equipped with such a false pixel irregularity pattern P, in the pixel field 20 and the seal field 227 at least, the surface surface smoothness of high degree of accuracy is realizable.

[0105] It is a thickness diagram -- thickness distribution of the 3rd interlayer insulation film 13 after the polish in the substrate 331 for liquid crystal panels which performed CMP processing is shown -- after drawing 16 forms the 3rd interlayer insulation film 13 by about 24000A of thickness in the operation gestalt 3 until the residual film thickness of the 3rd interlayer insulation film 13 of the core of the pixel field 20 becomes about 12000A. Moreover, the graph which puts the plot O mark in drawing 24 in a row shows distribution of the residual film thickness of the seal left part lengthwise direction which meets the a-a' line in drawing 16 . The graph which puts the plot O mark in drawing 25 in a row shows distribution of the residual film thickness of the pixel central lengthwise direction which meets the b-b' line in drawing 16 . The graph which puts the plot O mark in drawing 26 in a row shows distribution of the residual film thickness of the seal top chord longitudinal direction which meets the c-c' line in drawing 16 . The graph which puts the plot O mark in drawing 27 in a row shows distribution of the residual film thickness of the pixel central longitudinal direction which meets the d-d' line in drawing 16 , and the graph which puts the plot O mark in drawing 28 in a row shows distribution of the residual film thickness of the pixel central longitudinal direction which meets the e-e' line in drawing 16 .

[0106] As shown in these drawings, the maximum thickness difference in the pixel field 20 and the seal field 227 (seal four-corners section 227C is included) was about 850A, and the maximum thickness difference in the whole substrate was about 950A. The surface smoothness in the pixel field 20 and the seal field 227 was enough. In addition, in the perimeter field of the input terminal pad 26, since it is liable to polish lack somewhat, if the pattern consistency of the false pixel irregularity pattern P in the perimeter field of the input terminal pad 26 is lowered further, the further flattening is also realizable.

[0107] As a component which influences the concavo-convex configuration pattern in a pixel, they are the light-shielding film 12 of opening of two open beams, the gate line 4 of the lowest layer wiring, the data line 7 of the 1st metal layer, source electrode wiring 7a and the junction wiring 10, and the 2nd metal layer, and opening 12for plug penetration a at field oxide 3. With the false pixel irregularity pattern P of this example, it is false gate line 4p of the 1st metal layer about the gate line 4 of the lowest layer wiring. Although selected, it is false gate line 4p like the pixel field 20. You may form with the lowest layer wiring. Moreover, formation may be included for opening for false plug penetration assumed as false opening and opening 12a for plug penetration which were likened with opening of two open beams at field oxide 3 in the component of the false pixel irregularity pattern P. Since process use can be performed, a manday addition cannot be caused, but a much more real false pixel irregularity pattern can be formed in the outside of the pixel field 20, and further flattening of the pixel field 20 and the seal field 227 can be realized.

[0108] By the way, in CMP processing, it is hard to grind the first stage as the heights of a polished surface-ed being dense, and easy to grind the heights of a polished surface-ed conversely rough ******

and the first stage. It is because an isolated projection is ground quickly. Moreover, when the field as for which the projection of equivalent magnitude is carrying out random distribution densely, and the field which is carrying out random distribution to ** exist, since the direction of the field of ** has the quick initial polish rate, the inclination side over a both field may be formed by polish result. In the field of **, a pattern consistency is low as a result. on the other hand, the pattern consistency of which part of a polished surface-ed -- abbreviation -- even if equal, the direction of the field where the flat-surface magnitude (island-like area) of a projection is small has a quick initial polish rate. It is because it compares with island-like area and perimeter [the shape of an island] (profile) die length becomes long. Therefore, it is the hardest to grind the field the island-like area of a projection is carrying out [the field] random distribution greatly and densely the first stage. The ultimate example is the case where the continuous extension side (so-called solid) is formed in the whole field. On the contrary, it is the easiest to grind the field as for which the island-like area of a projection is carrying out random distribution to ** small the first stage. It is the case where a projection does not have the ultimate example in the whole field (there is no dummy pattern). However, although the field as for which the island-like area of a projection is carrying out random distribution to ** greatly, and the field over which the island-like area of a projection is distributed small and densely are the middle initial polish rates of the above-mentioned highest polish rate and the minimum polish rate The field as for which the island-like area of a projection is carrying out random distribution to ** greatly, and the field as for which the island-like area of a projection is carrying out random distribution small and densely Since it originates in polish liquid or other conditions (the regularity of distribution, a projection configuration, a projection array, projection arrangement, etc.), it is not [whether which one is a quick initial polish rate] ascertained. However, in actual CMP processing, since it is thought that the abrasive liquid has caused to some extent regular floating distribution by regular distribution of the irregularity of the pixel field 20, it is necessary to devise so that it may become the same floating distribution also in a non-pixel field.

[0109] Since the input terminal pad 26 is considered to be distribution of ** by the largest island-like projection in the chip size of the substrate for reflective mold liquid crystal panels, considering spacing of that one-dimensional array, the field containing this input terminal pad 26 actually serves as the highest polish rate. However, in the pixel field 20, the pixel irregularity pattern is presenting the clear space periodicity developed by two-dimensional [in every direction] in the shape of a matrix. Therefore, the hierarchical regulation which consists of the high order regularity of the space periodicity of a pixel irregularity pattern and the regularity of a low degree in a pixel irregularity pattern exists in concavo-convex distribution of the pixel field 20. A pixel irregularity pattern various kinds of microscopic basic (1st order) irregularity sections (field oxide 3 -- opening of two open beams, the gate line 4 of the lowest layer wiring, the data line 7 of the 1st metal layer, and source electrode wiring 7a --) represented by the detailed line breadth of 1000A - about 10000A And it is considered the layered structure which consists of the light-shielding film 12 of the junction wiring 10 and the 2nd metal layer, distribution of opening 12a for plug penetration, and the concavo-convex high density section (secondary irregularity sections) produced according to the bias of these basic irregularity section in a pixel. They are false gate line 4p, false data-line 7p, and false source electrode wiring 7ap so that the concavo-convex macro high density section may be selected instead of imitating the primitive basic irregularity section made to correspond to this basic irregularity section faithfully in detail by the false pixel irregularity pattern P of this example as it is. And false junction wiring 10p It forms. As the concavo-convex high density section of this example, the lap part of the gate line 4 and data 7 and the lap parts of capacity electrode 9a and the junction wiring 10 can be considered. For this reason, the false pixel irregularity pattern P is false gate line 4p and false data-line 7p. And false junction wiring 10p Containing is desirable. What is necessary is just to let a typical concavo-convex part be the element of the false pixel irregularity pattern P. The location of the typical concavo-convex part in the inside of the false pixel irregularity pattern P and the typical concavo-convex partial location in a actual pixel may not support accuracy.

[0110] Probably the minute DETTO copy of the basic irregularity section will not be required, and it will

be enough as it just to imitate even from a macroscopic hierarchy to the 3rd secondary irregularity sections, when for example, a pixel irregularity pattern is considered to be the 3rd more than layered structure here. However, when the layered structure of the concavo-convex pattern in such a pixel is not clear, there is an advantage to which the direction which uses the dead copy of the basic irregularity section as the false pixel irregularity pattern P can avoid the complicatedness on a mask design. Moreover, it is better to use the dead copy of a pixel as the false pixel irregularity pattern P, when planning flattening of further high degree of accuracy from which the maximum thickness difference becomes 1000A or less.

[0111] In addition, although it is suitable to use the liquid crystal panel substrate of the above-mentioned operation gestalt for a reflective mold liquid crystal panel, the reflective mold liquid crystal panel is applicable to the display of the display of pocket mold information processing machines, such as wrist watch mold electronic equipment, a word processor, and par SONARUKO pewter, and a portable telephone, or various kinds of electronic equipment in addition to this not to mention the light valve of a liquid crystal projector mentioned above.

[0112] Moreover, although the liquid crystal panel substrate of the above-mentioned operation gestalt makes a switching element to the principal plane of a semi-conductor substrate, not only as a semi-conductor substrate but as a substrate, insulating substrates, such as a glass substrate and a quartz substrate, can be used. Even when forming a thin film transistor (TFT) etc. on an insulating substrate as a switching element, it is not necessary to say that this invention is applicable.

[0113] Furthermore, this invention is applicable not only to a liquid crystal panel substrate but other substrates for a flat display.

[0114]

[Effect of the Invention] As explained above, this invention is characterized by the point which the dummy pattern was wedged into the crevice between pixel fields, and did not form in it, but applied the established conductive layer layer to reverse in the non-pixel field, and formed the dummy pattern for bottom raising of the interlayer insulation film of the upper layer of a ground layer in the abbreviation whole surface target. If the membrane formation process of the medium conductive layer for bottom raising and an interlayer insulation film must be added and the surface relief of the interlayer insulation film before polish is stopped, when forming a dummy pattern in a pixel field, since an initial polish rate will become low on the contrary, polish time amount required in order to carry out flattening of the interlayer insulation film front face to the mirror plane becomes long, and consumption of an abrasive liquid also increases. However, this invention does so about [that the above-mentioned inconvenience is cancelable] and the following effectiveness.

[0115] (1) When it has the dummy pattern of a monolayer or a double layer near the terminal pad, in order that the membrane formation surface level of the interlayer insulation film of the upper layer near the terminal pad may turn into the membrane formation surface level and abbreviation equivalent level in a pixel field and surface level may equalize as a whole, a uniform polish rate is obtained in polish processing. For this reason, the ******** of the terminal pad section which had become a problem in the condition that old membrane formation surface level is not equalized is improved, and the substrate of the terminal pad section is not exposed. This is useful to flattening of the further mirror plane of a pixel field front face, and can also realize thin film-ization of the interlayer insulation film before polish processing. Since the aspect ratio of the contact hole of the current carrying part between layers in a pixel field is improvable with this thin film-ization, it can connect to narrow diameter-ization of opening by narrow diameter-ization of a contact hole. So, the protection-from-light engine performance improves and a switching element property can be improved. Of course, it is not necessary to cause the addition of membrane formation manday.

[0116] And if the near region of the terminal pad outside a pixel field is also covered with the dummy pattern of a conductive layer, since this dummy pattern will also serve as a light-shielding film, the stray light stops easily being able to go into the component field made from the outside of a pixel field to the

substrate, can control a photocurrent, and is useful to an improvement of a switching element.
[0117] (2) When the dummy pattern arranged around an input terminal pad consists of two or more subdivision dummy patterns subdivided superficially, the short circuit between adjoining terminal pads can be prevented, equalizing the surface level of the interlayer insulation film immediately after membrane formation.
[0118] (3) When between phase next door **** input terminal pads is a non-dummy pattern space, the short circuit between input terminal pads can be prevented certainly.
[0119] (4) When coming to set up spacing of this input terminal pad and the subdivision dummy pattern arranged to that perimeter more widely than spacing of wiring and the dummy pattern of that near, bridge formation with the input terminal pad and subdivision dummy pattern by the conductive particle of the anisotropy electric conduction film stops being able to happen easily, and a short circuit can be prevented as much as possible.
[0120] (5) When spacing of a junction terminal pad and the dummy pattern arranged to the perimeter is set up more widely than spacing of wiring and the dummy pattern of the near, on a junction terminal pad, a flow is usually achieved with a silver paste, but even if a silver paste overflows a junction terminal pad a little, it is hard coming to short-circuit to the dummy pattern of the near.
[0121] (6) In case polish processing performs flattening since the front face of the interlayer insulation film before polish processing of the part becomes it of a pixel field, and an abbreviation EQC when the dummy pattern is formed in the seal field which encloses the perimeter of not only the near region of a terminal pad but a pixel field, polish advances at a rate with a pixel field uniform to the periphery. For this reason, a reflection factor not only improves, but compared with old, the surface smoothness of a pixel field becomes much more good, and it becomes easy to determine the etching time of the contact hole after polish.
[0122] (7) Furthermore, this field becomes the upper surface level and the upper surface EQC of an interlayer insulation film of a seal field part by preparing a dummy pattern also in the periphery section of a seal field. Therefore, when it grinds, the interlayer insulation film front face of a seal field does not turn into an inclination side, and the adhesion of a sealant can be improved.
[0123] (8) When the dummy pattern of a seal field stacks on the pattern isolated in the control wiring layer and this layer of a switching element, is added and changes, flattening of the surface level of the interlayer insulation film of polish processing can be adjusted still more minutely.
[0124] (9) And it is arranged around a pixel field, and when a dummy pattern is accumulated on the near field of the actuation circuit which supplies a signal to a switching element and it grows into it, it is useful to flattening of the interlayer insulation film of polish processing etc.
[0125] (10) Furthermore in this invention, the dummy pattern is formed in the corner field of the seal field which encloses a pixel field by low distribution of a consistency rather than the side field of a seal field, or the boundary region of the corner concerned. For this reason, if the front face of the interlayer insulation film before the polish in the seal four-corners section is presenting the Men granularity which the irregularity by two or more discrete dummy patterns reflected and polish processing is performed Since it compares with boom hoisting near the flatness of the side section of a seal field and the initial polish rate of the four-corners section becomes quick, it goes on with the inclination in which the polish rate of the seal field inside surrounded in the four-corners section by the form dragged by this carries out abbreviation equalization, and the residual-film-thickness variation of a pixel field and a seal field is controlled.
[0126] (11) Moreover, since the corner field fell and the boundary part has started even when there is no dummy pattern in the seal four-corners section (pattern consistency zero), in early stages of polish, the boundary part serves as an inclination side, and the inclination side affects the method of inside gradually.
[0127] Therefore, overall flattening of a pixel field and a seal field can be obtained.
[0128] (12) and in this invention, the dummy pattern of a continuous extension side (so-called solid) is

formed in a non-pixel field again -- coming out -- there is nothing and the configuration in which two or more false pixel irregularity patterns which imitated the irregularity of a pixel were formed can be adopted. Since the surface irregularity pattern of a pixel and the surface irregularity pattern of almost resemblance have spread also on front faces other than the pixel field of the interlayer insulation film before polish processing, as soon as a polish rate spreads abbreviation etc. on them in every part of a substrate from the first stage, in a pixel field and a seal field at least, the surface surface smoothness of high degree of accuracy is realizable.

[0129] (13) With the configuration which repeated two or more false pixel irregularity patterns in the two-dimensional direction on the non-pixel field, and carried out expansion formation, since space regularity, such as the shape of a matrix of a pixel field, will also correspond, the surface surface smoothness in a pixel field and a seal field becomes remarkable.

[0130] (14) Since it becomes the pattern which bears most a close resemblance [regularity / of a part with the remarkable (typical) irregularity of a pixel, or a pixel field / concavo-convex] when this false pixel irregularity pattern consists of a false gate line and the false data line at least and changes, flattening of the interlayer insulation film in a pixel field and a seal field can be carried out to high degree of accuracy.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the top view showing the example of a layout configuration of the substrate for reflective mold liquid crystal panels of the reflective mold liquid crystal panel concerning the operation gestalt 1 of this invention.

[Drawing 2] It is the cutting plane showing the condition of having cut along with the B-B' line in drawing 1 .

[Drawing 3] It is the sectional view showing the condition of having changed the structure of a terminal pad to the cross-section structure of drawing 2 .

[Drawing 4] It is the part plan showing the neighborhood of a pixel field and a seal field in the substrate for reflective mold liquid crystal panels of the operation gestalt 1.

[Drawing 5] It is the part plan showing the neighborhood of a data-line actuation circuit in the substrate for reflective mold liquid crystal panels of the operation gestalt 1.

[Drawing 6] It is the part plan showing the neighborhood of a terminal pad in the substrate for reflective mold liquid crystal panels of the operation gestalt 1.

[Drawing 7] It is the part plan showing the connection condition of the terminal pad and flexible TEBU electric wire in the substrate for reflective mold liquid crystal panels of the operation gestalt 1.

[Drawing 8] It is the cutting plane showing the condition of having cut along with the A-A' line in drawing 7 .

[Drawing 9] It is the part plan showing the neighborhood of a junction terminal pad in the substrate for reflective mold liquid crystal panels of the operation gestalt 1.
[Drawing 10] It is a thickness diagram that thickness distribution of the 3rd interlayer insulation film after the polish in the substrate for liquid crystal panels which performed CMP processing is shown etc. after forming the 3rd interlayer insulation film by about 24000A of thickness in the operation gestalt 1 until the residual film thickness of the 3rd interlayer insulation film of the core of the pixel field becomes about 12000A.
[Drawing 11] It is the part plan showing the neighborhood of the four-corners section of a seal field in the substrate for reflective mold liquid crystal panels concerning the operation gestalt 2 of this invention.
[Drawing 12] It is the sectional view showing the condition of having cut along with the C-C' line in drawing 11 .
[Drawing 13] It is a thickness diagram that thickness distribution of the 3rd interlayer insulation film after the polish in the substrate for liquid crystal panels which performed CMP processing is shown etc. after forming the 3rd interlayer insulation film by about 24000A of thickness in the operation gestalt 2 until the residual film thickness of the 3rd interlayer insulation film of the core of the pixel field becomes about 12000A.
[Drawing 14] It is the part plan showing the neighborhood of the four-corners section of a seal field in the substrate for reflective mold liquid crystal panels concerning the operation gestalt 3 of this invention.
[Drawing 15] It is the sectional view showing the condition of having cut along with the C-C' line in drawing 14 .
[Drawing 16] It is a thickness diagram that thickness distribution of the 3rd interlayer insulation film after the polish in the substrate for liquid crystal panels which performed CMP processing is shown etc. after forming the 3rd interlayer insulation film by about 24000A of thickness in the operation gestalt 3 until the residual film thickness of the 3rd interlayer insulation film of the core of the pixel field becomes about 12000A.
[Drawing 17] It is the outline block diagram showing a video projector as an example of the projection mold indicating equipment using the reflective mold liquid crystal panel as a light valve.
[Drawing 18] It is the sectional view showing a reflective mold liquid crystal panel.
[Drawing 19] It is the top view showing the substrate for reflective mold liquid crystal panels used for the conventional reflective mold liquid crystal panel.
[Drawing 20] It is the part plan showing the pixel field of the substrate for reflective mold liquid crystal panels of drawing 19 .
[Drawing 21] It is the cutting plane showing the condition of having cut along with the A-A' line in drawing 13 .
[Drawing 22] It is the cutting plane showing the condition of having cut along with the B-B' line in drawing 12 .
[Drawing 23] It is a thickness diagram that thickness distribution of the 3rd interlayer insulation film 13 after the polish in the substrate for liquid crystal panels which performed CMP processing is shown etc. after forming the 3rd interlayer insulation film by about 24000A of thickness in the conventional high reflective liquid crystal shown in drawing 19 until the residual film thickness of the 3rd interlayer insulation film of the core of the pixel field becomes about 12000A.
[Drawing 24] In the conventional example of drawing 23 , the operation gestalt 1 of drawing 10 , the operation gestalt 2 of drawing 13 R> 3, and the operation gestalt 3 of drawing 16 , it is the graph which shows distribution of the residual film thickness of the seal left part lengthwise direction which meets an a-a' line, respectively.
[Drawing 25] In the conventional example of drawing 23 , the operation gestalt 1 of drawing 10 , the operation gestalt 2 of drawing 13 R> 3, and the operation gestalt 3 of drawing 16 , it is the graph which shows distribution of the residual film thickness of the pixel central lengthwise direction which meets a b-b' line, respectively.

[Drawing 26] In the conventional example of drawing 23 , the operation gestalt 1 of drawing 10 , the operation gestalt 2 of drawing 13 R> 3, and the operation gestalt 3 of drawing 16 , it is the graph which shows distribution of the residual film thickness of the seal top chord longitudinal direction which meets a c-c' line, respectively.

[Drawing 27] In the conventional example of drawing 23 , the operation gestalt 1 of drawing 10 , the operation gestalt 2 of drawing 13 R> 3, and the operation gestalt 3 of drawing 16 , it is the graph which shows distribution of the residual film thickness of the pixel central longitudinal direction which meets a d-d' line, respectively.

[Drawing 28] In the conventional example of drawing 23 , the operation gestalt 1 of drawing 10 , the operation gestalt 2 of drawing 13 R> 3, and the operation gestalt 3 of drawing 16 , it is the graph which shows distribution of the residual film thickness of the pixel central longitudinal direction which meets an e-e' line, respectively.

[Description of Notations]

1 -- P -- Mold semi-conductor substrate
2 21' -- P type well field
3 -- Field oxide
4 -- Gate line
4a -- Gate electrode
4b -- Gate dielectric film
4p -- False gate line
5b--N+ Mold drain field
6 -- The 1st interlayer insulation film
6a, 6b, 6c, 16 -- Contact hole
7 -- Data line
7a -- Source electrode wiring
7p -- False data line
7ap(s) -- False source electrode wiring
8 -- P type capacity electrode field
9a -- Capacity electrode
9b -- Insulator layer (dielectric film)
10 -- Junction wiring
11 -- The 2nd interlayer insulation film
12 -- Light-shielding film
12a -- Opening for plug penetration
12b -- Wiring for connection
12p -- False light-shielding film
13 -- The 3rd interlayer insulation film
14 -- Pixel electrode
15 -- Connecting plug (current carrying part between layers)
17 -- Passivation film
20 -- Pixel field (viewing area)
21 -- Data-line actuation circuit (X driver)
22R, 22L -- Gate line actuation circuit (Y driver)
23 -- Precharge and test circuit
24 -- Picture signal sampling circuit
25 -- Light-shielding film
26 26' -- Input terminal pad
26a -- Lower layer
26b, 26b' -- Upper layer

27,127,227 -- Seal field
29R, 29L -- Junction terminal pad (fish eye)
30 -- Reflective mold liquid crystal panel
31,131,231,331 -- Substrate for reflective mold liquid crystal panels
32 -- Support substrate
33 -- Counterelectrode (common electrode)
35 -- Glass substrate
37 -- Liquid crystal
38 -- Anisotropy electric conduction film (ACF)
38a -- Conductive particle
38b -- Insulating resin material for adhesion
39 -- Flexible tape wiring
39a -- Flexible tape
39b -- Electric conduction line
100 -- Polarization lighting system
110 -- Integrating lens
127a -- Pattern
127C, 227C -- Four-corners section
130 -- Polarization sensing element
200 -- Polarization beam splitter
201 -- S polarization bundle reflector
261 -- Electric conduction contact section
262 -- Wiring cash-drawer section
412,413 -- Dichroic mirror
300B, 300R, 300G -- High-reflective-liquid-crystal light valve
500 -- Projection optical system
600 -- Screen
L0 -- System optical axis
A -- Lower layer dummy pattern
B, B' -- The upper dummy pattern
a -- Subdivision dummy pattern
X, X', Y -- Hazama field
W -- Line writing direction wiring field
L, LIN, and LOUT -- Wiring
M, T -- Dummy pattern between wiring
NR and NL -- Dummy pattern
S0, S1, S2, and S2 ' and S3 -- Subdivision dummy pattern
P -- False pixel irregularity pattern

[Translation done.]